RF PLANAR SWITCH AT KU BAND FOR MOBILE SATELLITE COMMUNICATIONS

VINÍCIUS LISBOA DO NASCIMENTO

DISSERTAÇÃO DE MESTRADO EM ENGENHARIA ELÉTRICA
PROGRAMA DE PÓS-GRADUAÇÃO EM ENGENHARIA ELÉTRICA

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CHAVEADOR PLANAR RF EM BANDA KU PARA COMUNICAÇÕES MÓVEIS POR SATÉLITE

VINÍCIUS LISBOA DO NASCIMENTO

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DISSERTAÇÃO DE MESTRADO SUBMETIDA AO DEPARTAMENTO DE ENGENHARIA ELÉTRICA DA FACULDADE DE TECNOLOGIA DA UNIVERSIDADE DE BRASÍLIA COMO PARTE DOS REQUISITOS NECESSÁRIOS PARA A OBTENÇÃO DO GRAU DE MESTRE.

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Dedico a minha família, principalmente a minha mãe que sempre me apoiou

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ABSTRACT

Title: RF Planar Switch at Ku band for Mobile Satellite Communications
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Brasília, June 30th, 2022

The presented dissertation describes the course of development of an RF switch designed to operate in the Ku band. This circuit is part of a much bigger project. The central system is a Ku band transceiver with a beamformer. The beamformer comprises a switch matrix, a set of RF planar lenses, and an antenna array. The RF switch needed a low insertion loss, high insulation between ports, low return loss, and high incident power. At first, research was done to verify the state-of-the-art RF switches and the available products that meet the requirements. After noticing that none of them were applicable, several versions of switches were made for this specific purpose and compared to which design was the best for this objective. Both PIN diodes and FETs were used. These circuits were developed and simulated for a microstrip design for possible future large-scale manufacturing. There were several complications in the design, optimization, fabrication, biasing, and testing. From microstrip lines erupting in the manufacturing process to errors during bias of the diodes. As some designs led to failures, the switch versions were improved and also simplified, sacrificing bandwidth and power handling. In addition, more prominent microstrip lines were used, the substrate was changed to use more common processes, and biasing tests were made to assure the proper functionality of the circuit. The ultimate version was an SP4T FET switch operating at lower Ku band (11.7 to 12.2 GHz) simulated with good results but yet to be tested (due to the pandemic crisis). A Rotman lens was also designed with seven beam ports and eight array ports. The lens was simulated with the simulated results of the SP4T to check the functionality of the beam steering system. The results show the beam direction change corresponding to the lens port selected by the RF switch as planned ($0°$, $\pm 10°$, $\pm 20°$, $\pm 30°$). After all, the system (RF switch and Rotman lens) worked well at the simulation level but still needs to be tested separately and together.

Keywords: rf switch, beam steering, ku-band, satellite communication.

RESUMO

Título: Chaveador planar RF em Banda Ku para Comunicações Móveis por Satélite
Autor: Vinícius Lisboa do Nascimento
Orientador: Sebastien Rondineau
Programa de Pós-Graduação em Engenharia Elétrica
Brasília, 30 de junho de 2022

A dissertação apresentada descreve o curso de desenvolvimento de um *switch* RF projetado para operar na banda Ku. Este circuito faz parte de um projeto muito maior que consiste em um sistema transceptor de banda Ku com um formador de feixe. O formador de feixe compreende uma matriz de chaveadores, um conjunto de lentes planares RF e um arranjo de antenas. O chaveador RF tem como requisitos: baixa perda de inserção, alto isolamento entre as portas, baixa perda de retorno e alta potência incidente. Em um primeiro momento, foram feitas pesquisas para verificar os chaveadores RF do estado da arte e os produtos disponíveis que atendem aos requisitos. Após constatar que nenhum deles era aplicável, várias versões de chaveadores foram feitas para esse fim específico e comparadas com qual projeto era o melhor para esse objetivo. Ambos os diodos PIN e FETs foram usados. Esses circuitos foram desenvolvidos e simulados para um projeto de microfita sobre substrato para possível futura fabricação em larga escala. Houveram várias complicações no projeto, otimização, fabricação, polarização e teste. Desde linhas de microfitas em erupção no processo de fabricação até erros durante a polarização dos diodos. Como alguns projetos levaram a falhas, as versões do switch foram aprimoradas e também simplificadas, sacrificando largura de banda e potência manipulada. Além disso, foram usadas linhas de microfitas mais largas, o substrato foi alterado para usar processos mais comuns e foram feitos testes de polarização para garantir a funcionalidade adequada do circuito. A versão final é a de um switch SP4T FET operando em banda Ku inferior (11,7 a 12,2 GHz) simulado com bons resultados, mas ainda a ser testado (devido à crise da pandemia). Também foi projetada uma lente de Rotman com sete portas de feixe e oito portas de arranjo. A lente foi simulada com os resultados simulados do SP4T para verificar a funcionalidade do sistema de direcionamento de feixe. Os resultados mostram a mudança de direção do feixe correspondente à porta da lente selecionada pelo switch RF conforme planejado ($0°$, $\pm 10°$, $\pm 20°$, $\pm 30°$). Ao final, o sistema (*switch* RF e lente de Rotman) funcionou bem no nível de simulação, mas ainda precisa ser testado separadamente e em conjunto.

Palavras-chave: chaveador RF, direcionamento de feixe, banda ku, comunicação por satelite.

SUMMARY

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LIST OF SYMBOLS

Greek symbols

Γ	Reflection coefficient	
Ω	Ohm	
β	Phase progression	[rad]
δ_0	Minimum transmission line length	[m]
δ_N	Excess length for port N	[m]
λ	Wavelength	[m]
ω	Angular frequency	[rad/s]
ϕ	Elevation angle	[rad | °]
σ_N	Length of transmission lines giving access to antenna N	[m]
τ_m	Switching time	[s]
ε_s	Electrical permittivity constant of a substrate	[F/m]
ϕ_s	Beam angle	[rad | °]
θ	Azimuth pointing angle	[rad | °]

Latin symbols

C	Capacitance	[F]
C_j	Diode junction capacitance when reverse biased	[F]
C_{OFF}	Capacitance for a reverse biased control element	[F]
E_m	Breaking electric field	[V/m]
E_{Total}	Electric field from the antenna array	[V/m]
$E_{element}$	Electric field from an antenna	[V/m]
I_i	Fourier coefficient, at the fundamental frequency, for the current at the port i	[A]
I_j	Fourier coefficient, at the fundamental frequency, for the current in the port j	[A]
I_{load}	Current over load	[A]
L_i	Characteristic inductance of the diode	[H]
P_1	Signal power on port 1	[W]
P_2	Signal power on port 2	[W]
P_A	Power available to the load from the source	[W]
P_m	Maximum power	[W]
P_{REF}	Reflected power	[W]
P_{load}	Power over load	[W]
R_f	Resistance of the forward biased diode	[Ω]

R_r	Resistance of the reverse biased diode	[Ω]
R_{OFF}	Resistance for a reverse biased control element	[Ω]
R_{ON}	Resistance for a forward biased control element	[Ω]
S_{ij}	Scattering parameter from port j to port i	
V_B	Breakdown voltage	[V]
V_F	Forward bias voltage	[V]
V_g	Source peak voltage	[V]
V_i	Fourier coefficient, at the fundamental frequency, for the voltage at port i	[V]
V_j	Fourier coefficient, at the fundamental frequency, for the voltage at the port j	[V]
V_{REV}	Reverse polarization voltage	[V]
V_{RMS}	Effective voltage	[V]
V_{load}	Voltage on load	[V]
W	Diode channel width	[μm]
Z_0	Characteristic impedance	[Ω]
Z_f	Forward biased diode impedance	[Ω]
Z_r	Impedance of the reverse biased diode	[Ω]
Z_{0i}	Reference impedance on port i	[Ω]
Z_{0j}	Reference impedance on port j	[Ω]
Z_{CTL}	Control element impedance	[Ω]
Z_{load}	Load impedance	[Ω]
f	Frequency	[Hz]
f_c	Center frequency	[Hz]
k_0	Free space wave number	[m^{-1}]
F	Focal distance	[m]
Z_{cap}	Impedance of a capacitor	[Ω]
d_Y	Distance between antennas on the y axis	[m]
d_Z	Distance between antennas on the z axis	[m]
v_s	Switching speed for a PIN diode	[cm/s]
d	Distance between antennas for a linear array	[m]

Dimensionless symbols

A_j	Incident wave
B_i	Reflected wave
F_0	Focal point on the main axis
F_1, F_2	Focal points outside the lens
G	Bootlace lens main axis
M	Number of beam ports

R_{0i}	Real part of the reference impedance at port i
R_{0j}	Real part of the reference impedance at port j
Re	Real part
a_n	Excitation coefficient
x_N	Position on the x axis of radiant elements
x_{bM}	Position on the x axis of beam ports
x_{pN}	Position on the x axis of element ports
y_N	Position on the y axis of radiant elements
y_{bM}	Position on the y axis of beam ports
y_{pN}	Position on the y axis of element ports
N	Number of antennas in an array on an axis
j	Imaginary unit
$\tan\delta$	Tangent of losses of a substrate
$\mathbf{a}_N$	Antenna at position N of a linear array
$\mathbf{a}_{NM}$	Antenna at position NM of an array NxM

LIST OF ACRONYMS AND ABBREVIATIONS

ADS Advanced Design System by Keysight. 84
AF Array Factor. 9, 73, 84

BJT Bipolar Junction Transistor. 84
BW bandwidth. 5, 84

CW Continuous wave. 22, 84

DC Direct current. 27, 84
DFT Discrete Fourier Transform. xi, 9, 10, 84
DIP dual in-line package. 36, 84
DL Data Link layer/protocols. 84

EM Electromagnetism / Electromagnetic. 44, 84

FET Field effect transistor. 3, 84
FPGA Field Programmable Gate Array. 36, 84

GaAs Gallium arsenide. 84

HB Harmonic balance simulation from ADS. 84

IF Intermediate frequency. 4, 84
IL Insertion loss. 2, 22, 84
ISO Isolation. 2, 22, 84

JFET junction-gate field-effect transistor. 38, 84

LNA Low noise amplifier. 5, 84
LO Local oscillator. 5, 84
LSSP Large signal s-parameter simulation for ADS. 20, 84

MEMS Microelectromechanical system. 1, 84
mmWave Millimeter wave. 84
MoM Method of moments. 84

MSA Microwave switch array. 61, 84
MSM Microwave switch matrix. 1, 84

NF Noise Figure. 69, 84

PA Power amplifier. 22, 84
PCB Printed circuit board. xv, 50, 84
PPGEE Graduate Program in Electrical Engineering |*Programa de Pós-Graduação em Engenharia Elétrica*. 84

RADAR RAdio Detection And Ranging. 84
RF Radio frequency. 1, 84
RL Return loss. 22, 84
RX Reception. 84

SCUBA Self-Contained Underwater Breathing Apparatus. 84
SDR Software defined radio. 4, 84
SMA Subminiature version A. 49, 84
SMD Surface mounted components. 26, 84
SMP Subminiature push-on. 37, 84
SP2T Single-pole double-throw. 22, 84
SP4T Single-pole four-throw. 11, 84
SP6T Single-pole six-throw. 11, 84
SP8T Single-pole eight-throw. 11, 84
SPDT Single-pole double-throw. 23, 84
SPST Single-pole single-throw. 13, 84

TL Transmission line. 27, 84
TX Transmission. 84

UnB University of Brasilia | Universidade de Brasília. 84
UTI Unidade de Tratamento Intensivo. 84

VNA Vector Network Analyzer. 67, 84

WCNPS Workshop on Communication Networks and Power Systems. 8, 84

1 INTRODUCTION

Mobile transceivers are devices that transmit and receive signals from a geostationary satellite, which, in its turn, communicates with a fixed station. The transmitter transforms a digital signal to baseband, shifting it to higher frequencies and amplifying its power to deliver it to the radiating system. For the return link, the analog signal in Radio frequency (RF) is coming from the radiating system, amplified for having low power, and converted to baseband [15].

The radiating set, explained above, is a system that allows the transfer of signals through air or vacuum in the form of electromagnetic waves. The architecture of the system is composed of an array of phased antennas and a beam former. The antenna array consists of multiple radiant elements placed in a pattern [1].

The beamformer is composed of two parts: phase shifters (Rotman) – which are two-dimensional microstrip lenses on parallel planes, to feed the radiant elements [16] – and RF switches – devices capable of controlling the alternation of signals from antennas to receive or transmit information [17].

This system is promising because it raises the antenna gain, has a more collimated beam, and is more reliable mechanically, as it does not require movement [18]. On the other hand, its beam formation is more complicated, needing something that quickly selects which beam should be used together with a satellite pointing system [19].

The target was to research the technologies involved in the development of an RF switch and a Ku-band Microwave switch matrix (MSM) [20], and design a switch and MSM prototype. These designs needed to meet some requirements: fast transition between beams, and low insertion loss, considering the received signal is attenuated by free-space path loss and weather conditions for the mobile satellite terminal. It also pointed out the obstacles that affect the design of a switch for millimeter-wave.

1.1 STATE-OF-THE-ART

A search was done for technologies available on the market regarding microwave switching signals. This research involved journals, databases, and several national and international manufacturers and products. It also involved the possible development of a switch from zero.

Two types of technologies were found for millimeter-wave switches: Microelectromechanical system (MEMS) and solid-state. MEMS type switches are an emerging technology

with many attractive qualities, but there are still difficulties. Because it is a component with mechanical parts, its reliability and quality packaging are affected [8].

Solid-state switches are generally more reliable and widely used on the market. In addition, they have a longer life cycle due to high resistance to mechanical shocks, which may consist of PIN diodes or transistors. It's also possible to achieve better transition speeds. However, they still have higher resistance when turned on, which increases insertion loss over those of the MEMS [8]. Other information was commented and developed in Section 2.2.

It was necessary to use transmission lines for both types of technologies, indicating the use of microstrip for better cost-benefit. Furthermore, it is easy to create a prototype and can be produced on a large scale in Brazil.

The most important technologies, parameters and characteristics are: frequency of operation, Insertion loss (IL), Isolation (ISO), switching time and power consumption. These are the basic aspects presented in the following table.

Table 1.1 – Comparison os state-of-art switches in different technologies [10]

Model	Max Freq. [GHz]	IL [dB]	ISO [dB]	Switching Time	Power Consumption
CMOS	300	1.5 - 7	20 - 66	> 550 ps	low
PIN	130	1.5 - 3.5	20 - 40	> 30 ns	high
MEMs	240	0.45 - 2	20 - 55	< 10 ns	low

This summary (Table 1.1) compiles the most important technologies and parameters for comparison. Beyond that, the topologies have a big part in the final result of a high-end switch. These topologies involve various styles, but the main ones are series, shunt, and hybrid. It directly impacts the loss and the isolation, affecting the overall performance.

1.2 JUSTIFICATION

The RF switch plays the role of switching between the desired ports, resulting in different directions. Therefore, the RF commutator is essential for the entire transmission chain to function. There are other technologies similar to those seen in Mailloux[18]. However, the switch was chosen by having a reduced value compared to others and having construction and logic more accessible for the steering system.

1.3 OBJECTIVE

1.3.1 General Objective

To identify commercial switches, technologies, and switch topologies applicable to an antenna array system and Ku-band mobile transceiver and develop an RF switch and switch matrix for this application.

1.3.2 Specific Objectives

- To analyze existing RF switch technologies;
- To analyze viable commercial Ku-band switches;
- To analyze and define switch topologies applicable to the project;
- To design and optimize an RF switch in electromagnetic simulation software;
- To design an RF switch matrix in electromagnetic simulation software.

1.4 DISSERTATION STRUCTURE

The work is organized in order to follow the development of the project. Chapter 2 exposes the knowledge needed to understand the project as a whole and the switch, such as explanations of the general project, transceivers, antenna array, Rotman lenses, control elements, RF switch topologies, Field effect transistors (FETs), and PIN diodes. The 3^{rd} chapter presents the methods for developing a switch and a matrix of RF switches in the Ku-band. Chapter 4 presents the results of the simulations of the circuits created and an analysis of what was done and manufactured. In the end, Chapter 5 summarizes what was developed during this dissertation and a brief comment on the results, findings, and limitations. The last chapter also points some suggestions for future works and testing.

2 REVIEW OF THE LITERATURE

It is necessary to understand the proposed system of which the switch is part beyond the knowledge of the RF switch itself.

2.1 PROJECT RATIONALE

The mobile terminal project encompasses several areas of knowledge and technology. Studies on the link, Link Budget, software-defined radio, integrated circuit, and RF circuitry are carried out.

The general system (Figure 2.1) consists of a Software defined radio (SDR) that takes the baseband signal to the Intermediate frequency (IF) Transceiver System-on-chip. Subsequently, the RF Transceiver reaps the IF signal, increasing the frequency once more so that the Radiating System can transmit it.

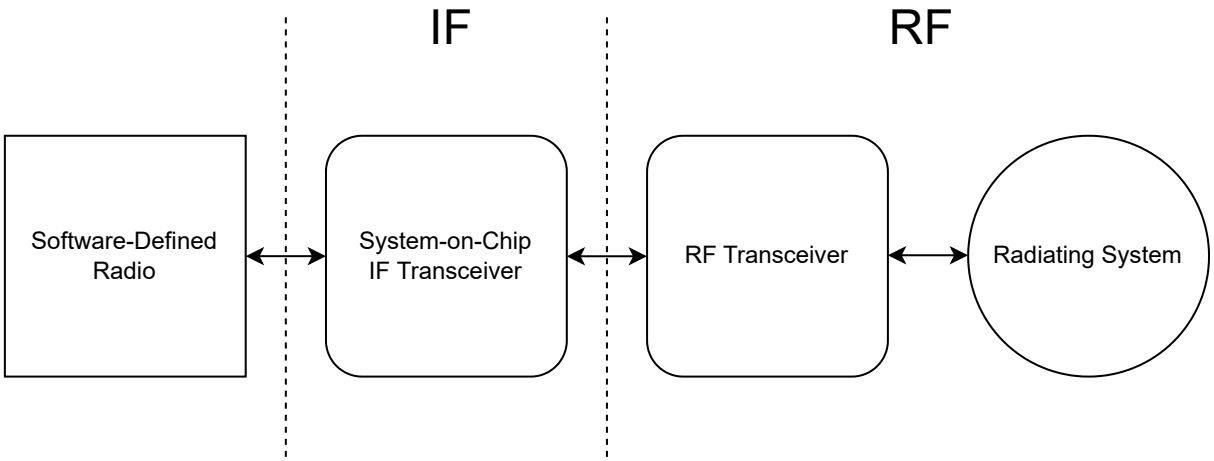

Figure 2.1 – Diagram of the overall system of the project showing the subsystems and the division of the signal into intermediate frequency and radiofrequency. Source: Own elaboration.

The same can be done for reception, where the signal is received from the satellite by the Radiating System, and the RF Transceiver reduces the frequency. Then, the signal on the IF Transceiver is frequency reduced again so that SDR can use it.

The RF switch is part of the RF part of the project (Figure 2.2) that mainly rely on the transceiver, the radiating system, and the like that constitute them (array of antennas, Rotman lens, and switch) and will be described in the following sections.

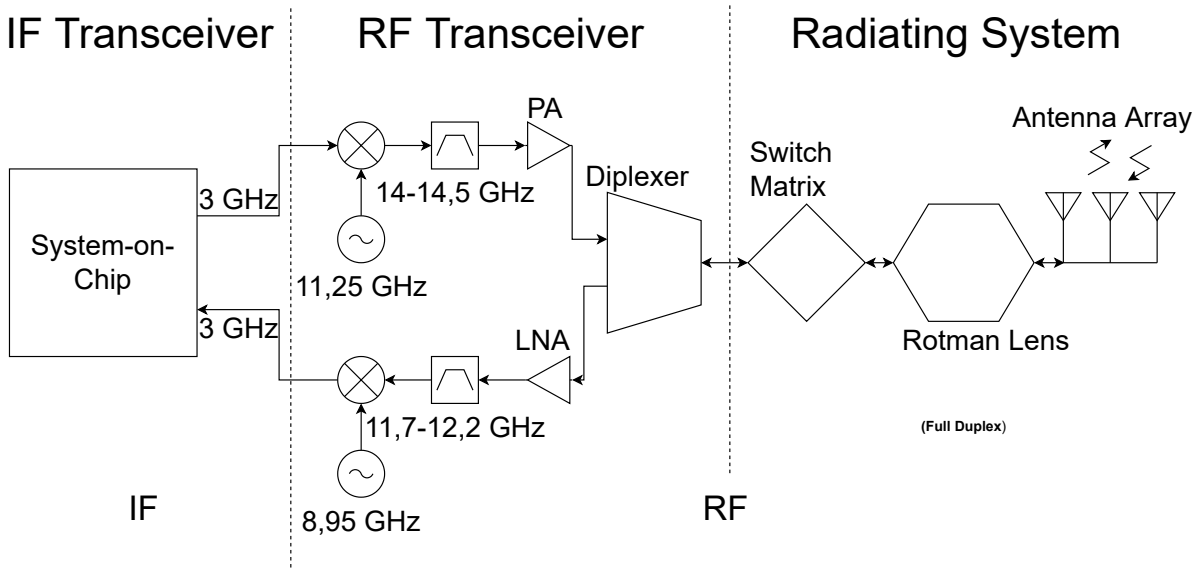

Figure 2.2 – Diagram of the overall full duplex system of the project showing the IF transceiver, RF transceiver, and the radiating system with its subsystems. Source: Own elaboration.

2.1.1 Overview of a Transceiver

One of the main parts of a mobile telecommunications terminal is the transceiver, a system containing simultaneously transmitter and receiver. In this platform, the receiver receives and transforms signals from antennas into signals that can be converted digitally. On the other hand, the transmitter converts the baseband signal to an intermediate frequency, later to the same used by the satellite to be delivered to the antennas.

The transceiver (Figure 2.3) must operate in the Ku band – transmit between $14\,\text{GHz}$ and $14,5\,\text{GHz}$ and receive between $11,7\,\text{GHz}$ and $12,2\,\text{GHz}$. The channels bandwidth (BW) must be $50\,\text{MHz}$ and can be changed across the entire $500\,\text{MHz}$ band.

The first stage converts a baseband signal to IF (inter-frequency average) of $3\,\text{GHz}$. The second stage raises this frequency with local oscillators and a mixer, passing through a filter in the band intended for transmission in the Ku band. Then the signal is boosted by a power amplifier so that the information is delivered to the satellite from kilometers away.

Due to the significant attenuation of the signal at reception (about $-110\,\text{dBm}$), the same receives a gain when passing through the Low noise amplifier (LNA) and is later filtered in the Ku-band reception range. Finally, the signal passes through a mixer to have its frequency reduced to around $3\,\text{GHz}$ with the help of aLocal oscillator (LO) at the frequency of $8.95\,\text{GHz}$. So the bits can be processed by an on-chip IF transceiver.

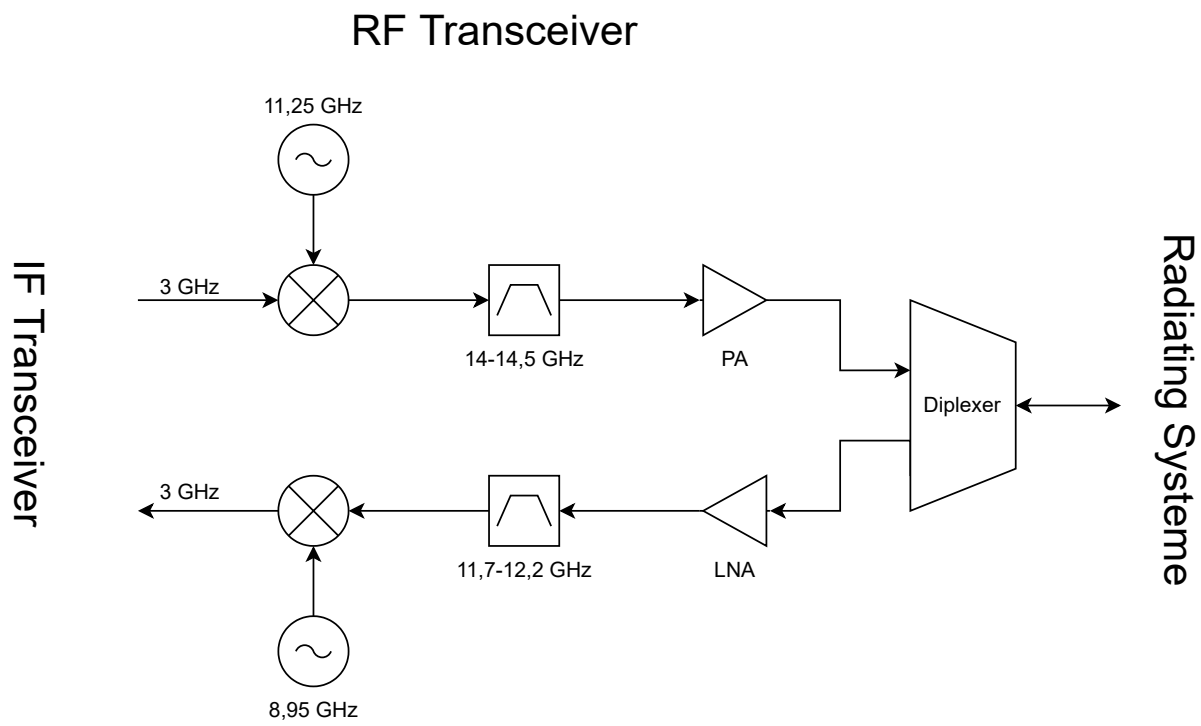

Figure 2.3 – Diagram of the design heterodyne RF Transceiver, showing its subcomponents with the transmission and reception path. Source: Own elaboration.

2.1.2 Radiating System

The Radiant System is a fundamental subsystem for the operation of the project. This is where the signal will be received and/or transmitted to the other subsystems. The current system consists of a horn antenna and a mechanical pointer that rotates tracking the direction of the satellite.

For the update made in the project, this subsystem (Figure 2.4) must be composed of a matrix of RF switches, Rotman lenses and the array of antennas.

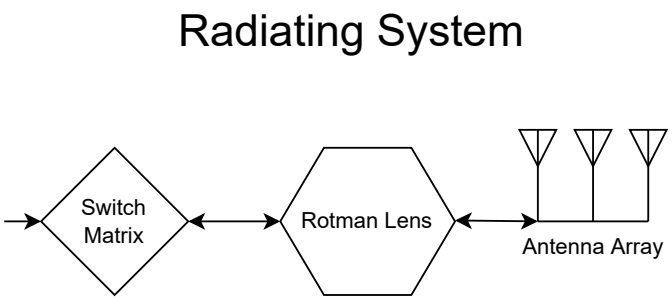

Figure 2.4 – Diagram of the project's radiating system showing the switch array, Rotman lens, and antenna array. Source: Own elaboration.

At the end of the project, the complete radiating system will have a switch matrix connected to a stack of vertical Rotman lenses, which will be connected to horizontal lenses and finally connected to the antenna array (Figure 2.5). This provides a pointing plane normal

to the pointing direction, resulting in the Rotman lens and the switch matrix determining the beam directions.

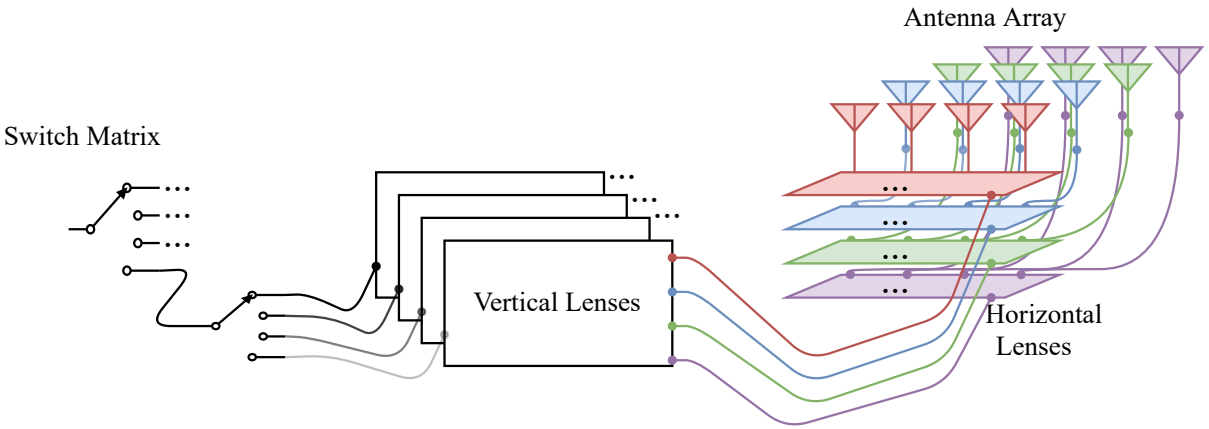

Figure 2.5 – A diagram of the project's radiating system shows the connection between matrix-lens, lens-lens, and lens-antenna array. Source: Own elaboration.

2.1.2.1 Antenna Array

An antenna is an element that transmits and receives electromagnetic energy. More usually, a single element is used that can have different parameters such as type, operating frequency, bandwidth, and gain, among other factors [21]. Nevertheless, sometimes the performance of a single antenna does not meet a particular demand.

According to Ma[22], the antenna array system is used for applications that require high gain, together with greater control of the main beam, as in the case of the transceiver project of the entity that finances the project. For the mobile communication terminal to be approved, the equipment must meet the established standards for radiated power and half-power beam opening, among others [23, 24]. The arrangement helps to meet these requirements and improve transmission.

Generally, the constituent elements of the array are identical and have the same orientation, but they can also be different from each other to achieve certain aspects. For example, a linear array of discrete elements (the most straightforward type) is a set of antennas spaced and arranged linearly (Figure 2.6a) behaving as a single antenna.

For an array, some of the most important aspects are the number of elements, the spatial arrangement, the irradiation pattern of the elemental antenna, and the phase excitation function. From there, the array parameters can be determined: array irradiation pattern, directivity, gain, and impedance [22].

Following the Figures 2.6a and 2.6b, in an array of N equally spaced elements of d the total electric field strength in the far field E_{Total} can be calculated as

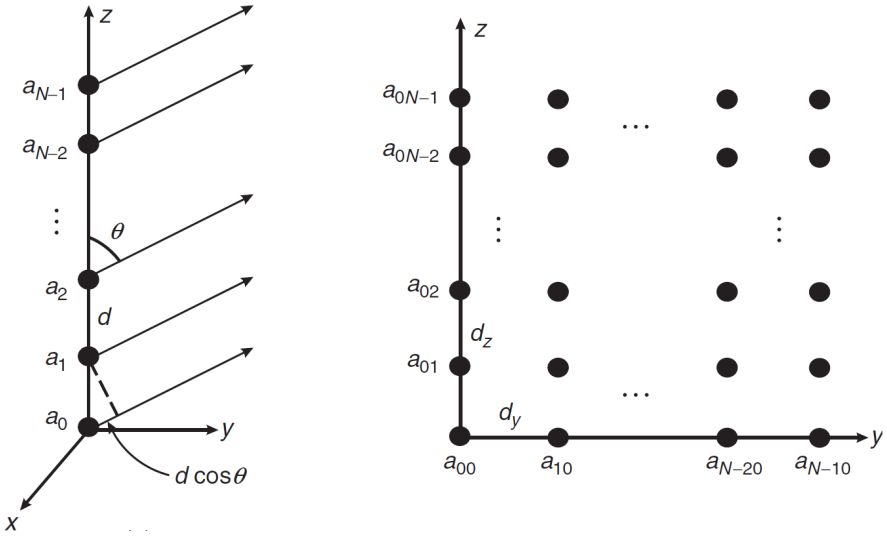

Figure 2.6 – Configuration of (a)Linear array $N \times 1$ with d spacing between elements and (b)Two-dimensional array $N \times N$ with horizontal spacing of d_Y and vertical d_Z between elements. Source: Volakis[1].

$$E_{Total} = E_{element}(\theta, \phi) \sum_{n=0}^{N-1} a_n e^{jn(k_0 d \cos\theta - \beta)} \tag{2.1}$$

, where $E_{element}$ is the electric field of a single element of the many that make up the array, a_n the amplitude of the individual element, k_0 the free space wavenumber, and β is the phase progression from one element to another [1].

For a direction with changes in elevation and azimuth – as required by the project – a two-dimensional array is needed (Figure 2.6b). In addition, something needs to change in the wavefront to direct the array's beam.

The radiating element and array used will likely be those created by Figueiredo e Nascimento[25] and presented during the 2019 Workshop on Communication Networks and Power Systems (WCNPS) with some modifications. This antenna array was composed by patch antennas in a 4 by 4 arrangement over a planar substrate.

2.1.2.2 Rotman Lens

A bootlace lens is a lens in which two arrays are accommodated on opposite sides utilizing transmission lines and phase shifters. The shape of the input and output elements, the length of the transmission line between them, and the phase weight determine the performance of the [2] lens.

Two-dimensional wide-angle microwave lenses, better known as Rotman lenses [26], are

a type of bootlace lens with three focal points – two off-axis (F_1 and F_2) and one on the main axis (G) – widely used by antenna arrays. They simultaneously form multiple beams for the antenna array.

On one side, M beam ports are arranged around the lens curve (called the focal curve) that transmit/receive to the opposite side of the Rotman lens for the array of N ports for the antenna array. The individual elements in this matrix are ordered linearly. Each beam port creates an array factor of the other array elements based on the geometry of the lens itself [2].

Figure 2.7 describes the variables that make up the Rotman lens. Among them is the angle of the wavefront $-\phi_s$ is the same as the angle of the source beam port of the signal. In this way, it is possible to cover M pointing angles for the linear array of N antennas.

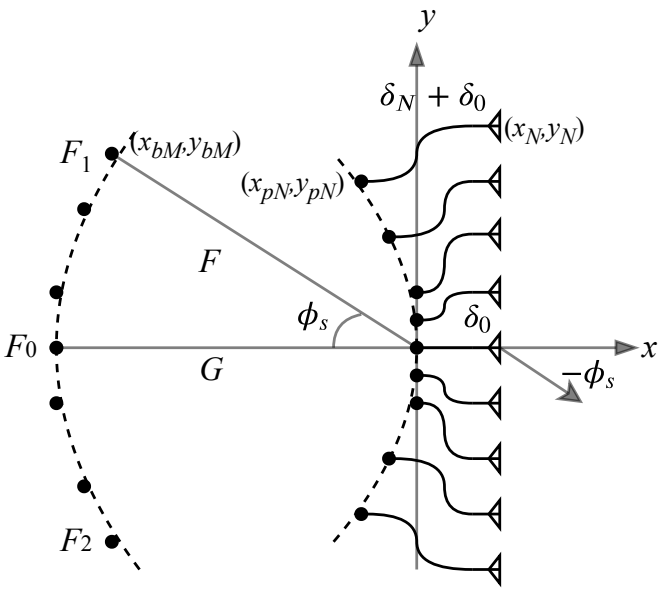

Figure 2.7 – Rotman lens diagram with M left beam ports and N right array ports connected to antennas arranged linearly by transmission lines. The diagram also shows the three foci F_0, F_1 and F_2, and the focal lengths G and F along with the beam angle ϕ_s and the lengths δ_N from the transmission lines. Source: Adapted from [2].

In short (Figure 2.8), the Rotman lens receives a planar wave from certain angle, samples it, phase-shifts it, window it and also recombines it. All of it is due to the Rotman lens geometry (port, focal arc, and lengths). It works basically as a DFT that generates an Array Factor (AF) closely to a gaussian curve at the desired angle.

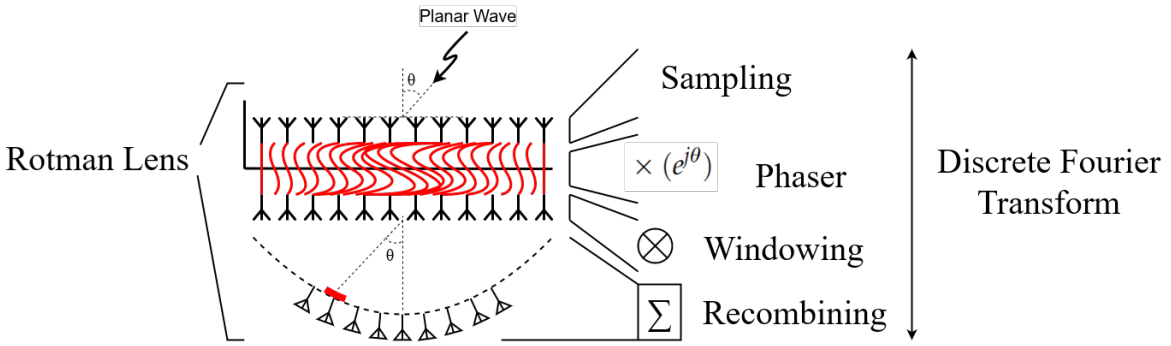

Figure 2.8 – Another Rotman lens diagram showing a comparison with the DFT. The lens ports sample the signal, which is offseted by the lens body. The signal also goes through windowing and over recombination due to the focal arc of the lens. That way most part of the energy is focused in the required direction (red part of the arche) with the same θ angle. Also shown on the lens is plane wave distortion (in red) which is smaller at the edges and larger in the center. Source: Own elaboration.

With the help of a switching mechanism, it is possible to change the beam angle in the desired direction. It is also possible, with interpolation, to track the position using the adjacent beams ([2]).

In addition to having a large frequency band (close to 3 GHz in width), the Rotman lens is a means of propagating the electromagnetic wave while, at its input and output, the phase is changed. In this way, it also changes the wavefront perceived by the system. Moreover, as there are no moving parts, it also proves to be a cheap and long-lasting alternative.

2.1.2.3 RF Switch Matrix

Switch arrays are widely used for communication systems, generally satellites, serving mainly as a router. For example, these arrays are already commercially used for products with smart antennas with switched beams.

The type of communication system to be used by the partner organization requires this matrix. The switches must select the strongest signal from the antennas to the receiver. For a small number of beams, it can use SPDTs (single-pole double-throw). It is used to describe a switch with one input and two outputs. Nevertheless, as this number increases, the more complicated the architecture of the MSM [27].

Figure 2.9 shows how these switches can be arranged in order to multiply the output that used to be two to 2^n outputs, corresponding to the n levels. So it is possible to achieve such a high number of beams.

In principle, for the radiating system being developed, up to 256 radiating elements will be used and up to 256 different directions. Therefore, up to 256 different beams must be fed by an equal number of ports that the switch matrix must reach.

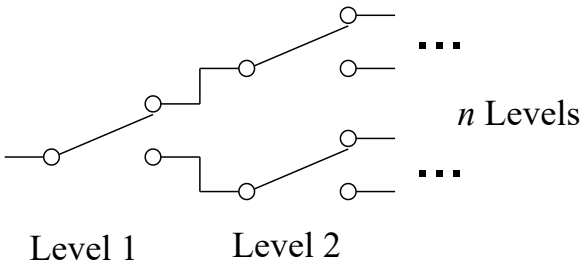

Figure 2.9 – Cascaded SPDT switches showing n levels exemplifying the assembly of an array of RF switches. Source: Own elaboration.

One of the concerns of cascading switches is the increase in insertion loss. According to U-yen, Dong e Kenney[27] there is a concern in large matrix architectures regarding IL(Insertion loss), in addition to routing problems that compromise isolation.

Thus, an exchange must balance the matrix losses by the number of levels and the number of beams generated by the radiating system. One way around this is to create a switch with more outputs (Single-pole four-throw (SP4T), Single-pole six-throw (SP6T), Single-pole eight-throw (SP8T)...). In this way, fewer levels will be needed and fewer switches.

2.2 RF SWITCH

According to Caverly[3], the primary switch concept involves the question of the location of the control element and its impedance in the control circuit. A low impedance for the ON state and a high impedance for the OFF state is required for series switching elements. A high impedance for on-state and a low impedance for off-state is required for switching elements in parallel.

For RF, there are two fundamental types of switches: solid-state and MEMS (Micro-electromechanical systems). MEMS are made up of mechanical elements that touch a fin, allowing, or not, the passage of the signal. In solid-state devices, semiconductors are used that change their internal impedance [3]. For solid-state, the control elements can be PIN diode, FET (field effect transistor), or hybrid (PIN and FET diode).

In MEMS-type elements, the impedance seen in its "ON" state by the source is equivalent to that of a conductor, that is, very low. For its "OFF" state, the impedance seen by the signal source is that of an open circuit, very high, with an addendum of a small capacitance created between the metal fin of the device.

For solid-state elements, voltage and current affect their operation. For example, in Figure 2.10a the element placed in series has an impedance Z_{CTL}, for example, in an impedance system Z_0 with matching between the source and the load.

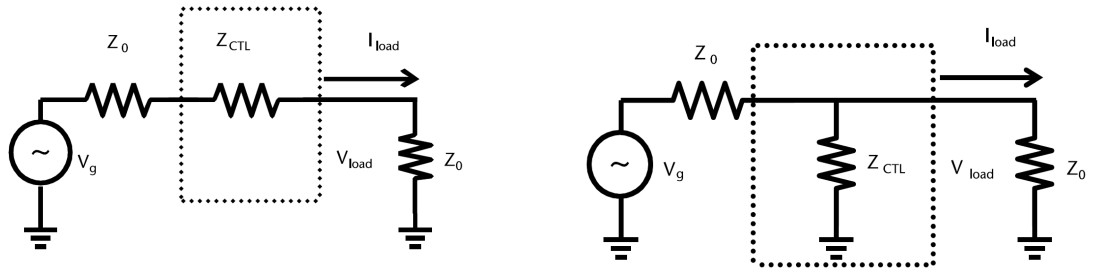

Figure 2.10 – Control element in (a)Series and in (b)Parallel. Dotted part representing control element as quadrupole. Source: Caverly[3].

For the impedances as mentioned earlier, the voltage and current at the load can be described by circuit analysis as

$$V_{load} = V_g \frac{Z_0}{2Z_0 + Z_{CTL}}, \tag{2.2}$$

$$I_{load} = V_g \frac{1}{2Z_0 + Z_{CTL}} = \frac{V_{load}}{Z_0}. \tag{2.3}$$

The power provided by the source is the same at the load in the absence of the control element and can be described as

$$P_A = \frac{V_g V_g^*}{8Z_0}, \tag{2.4}$$

where the voltage V_g is the peak voltage of the source and V_g^* its complex conjugate. The purely real load power, with the addition of the control device, is

$$P_{load} = \frac{1}{2}\,\mathrm{Re}(V_{load} I_{load}^*) = \frac{1}{2}\,\mathrm{Re}\left[\left(V_g \frac{Z_0}{2Z_0 + Z_{CTL}}\right)\left(V_g \frac{1}{2Z_0 + Z_{CTL}}\right)^*\right] = P_A \left|\frac{2Z_0}{2Z_0 + Z_{CTL}}\right|^2. \tag{2.5}$$

For a parallel control element (Figure 2.10b), an analysis similar to that done in series can be performed. The peak voltage and current can be calculated as

$$V_{load} = V_g \frac{Z_{CTL}}{2Z_{CTL} + Z_0}, \tag{2.6}$$

$$I_{load} = \frac{V_g}{Z_0} \frac{Z_{CTL}}{2Z_{CTL} + Z_0} = \frac{V_{load}}{Z_0}. \tag{2.7}$$

Load power for this type of configuration can also be calculated similarly. Soon

$$P_{load} = \frac{1}{2}\,\mathrm{Re}(V_{load} I^*_{load}) = \frac{1}{2}\,\mathrm{Re}\left[\left(V_g \frac{Z_{CTL}}{2Z_{CTL}+Z_0}\right)\frac{V_g^*}{Z_0}\left(\frac{Z_{CTL}}{2Z_{CTL}+Z_0}\right)^*\right] = P_A\left|\frac{Z_{CTL}}{2Z_{CTL}+Z_0}\right|^2. \tag{2.8}$$

In Equation 2.8 it is noted that for a small Z_{CTL} compared to Z_0, the value of P_{load} approaches zero. With a high Z_{CTL}, power is delivered to the load. Series and parallel elements work in inverse logic to each other.

In solid-state elements, what usually happens is the appearance of a small capacitance that raises the impedance of this same control element to high frequencies.

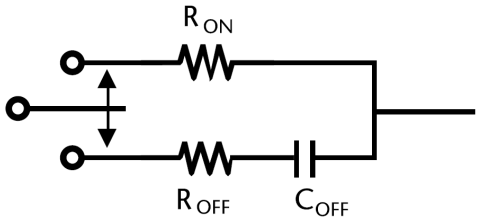

Figure 2.11 – The simplified schematic of the control element with different impedances. Above, R_{ON} impedance when allowing the signal to pass through ON. Below, impedances R_{OFF} and C_{OFF} when it does not allow the signal to pass in OFF. Source: Caverly[3].

When allowing current to flow, R_{ON} is the only impedance seen by the simplified system above (Figure 2.11). When current is not allowed, the impedances seen come from R_{OFF} and C_{OFF}.

2.2.1 Series Reflective Switch

One of the simplest switching circuits is the reflective type. It works by creating an impedance mismatch between the source and the load, reflecting the signal. This makes reflection coefficient analysis so important [3].

As the system is not perfect, part of the power of the source P_A is reflected by the impedance mismatch

$$P_{REF} = P_A \Gamma\Gamma^* = P_A|\Gamma|^2, \tag{2.9}$$

and the part arriving at the load can also be described as

$$P_{IN} = P_A(1 - |\Gamma|^2). \tag{2.10}$$

For a Z_0 impedance system with series control of Z_{CTL} impedance from a Single-pole

single-throw (SPST), the reflection coefficient seen by the source is

$$\Gamma = \frac{(Z_{CTL} + Z_0) - Z_0}{(Z_{CTL} + Z_0) + Z_0} = \frac{Z_{CTL}}{Z_{CTL} + 2Z_0}. \tag{2.11}$$

The Equation 2.11 can be used to calculate the reflection coefficients for the on (ON) and off (OFF) state of the switch, being

$$\Gamma = \frac{R_{ON}}{R_{ON} + 2Z_0} \qquad \text{ON,} \tag{2.12a}$$

$$\Gamma = \frac{R_{OFF} + 1/\mathrm{j}\omega C_{OFF}}{(R_{OFF} + 1/\mathrm{j}\omega C_{OFF}) + 2Z_0} \qquad \text{OFF.} \tag{2.12b}$$

In its ON state, the insertion loss IL in dB in the switch is calculated using equation 2.12a as

$$IL = 20\log_{10}\left(1 + \frac{R_{ON}}{2Z_0}\right). \tag{2.13}$$

In its OFF state, the ISO isolation in dB on the switch is calculated using the equation 2.12b as

$$ISO = 20\log_{10}\left|1 + \frac{R_{OFF} + 1/\mathrm{j}\omega C_{OFF}}{2Z_0}\right|. \tag{2.14}$$

Furthermore, the isolation for a reactance generated by C_{OFF} much larger than R_{OFF} can be simplified as

$$ISO = 10\log_{10}\left(1 + \frac{1}{(2\omega C_{OFF} Z_0)^2}\right). \tag{2.15}$$

2.2.2 Parallel Reflective Switch

Parallel Reflex Switch analysis can be done similarly to Section 2.2.1 for a switch SPST. The Z_{CTL} impedance seen in Figure 2.10b creates an impedance mismatch between the source and the load [3]. For an impedance system Z_0 with parallel control of impedance Z_{CTL}, the reflection coefficient seen by the source is

$$\Gamma = \frac{-Z_0}{2Z_{CTL} + Z_0}. \tag{2.16}$$

The previous equation can be used to calculate the reflection coefficients for the on (ON) and off (OFF) state of the switch, being

$$\Gamma = \frac{-Z_0}{2(R_{OFF} + 1/\mathrm{j}\omega C_{OFF}) + Z_0} \qquad \text{ON,} \tag{2.17a}$$

$$\Gamma = \frac{-Z_0}{2R_{ON} + Z_0} \qquad \text{OFF.} \tag{2.17b}$$

$$IL = 20\log_{10}\left|1 + \frac{Z_0}{2(R_{OFF} + 1/\mathrm{j}\omega C_{OFF})}\right|. \tag{2.18}$$

For very high reactance, R_{OFF} becomes almost negligible. The IL can then be simplified as

$$IL = 10\log_{10}\left(1 + \left(\frac{\omega C_{OFF} Z_0}{2}\right)^2\right). \tag{2.19}$$

In its OFF state, the ISO isolation in dB in the switch is calculated using the equation 2.17b as

$$ISO = 10\log_{10}\left(1 + \frac{Z_0}{2R_{ON}}\right). \tag{2.20}$$

2.3 PIN DIODE

One of the primary uses of diodes is switching devices, turning RF signals on and off, which generally demands considerable power. Its operation requires the diode to switch between two states. One with low impedance, which allows the signal to pass through, and one with high impedance, which blocks the signal [28]. For millimeter-wave signals, PIN diodes are used.

The PIN diode has an intrinsic layer inserted between the regions of type p and type n (Figure 2.12). The intrinsic region i has a low charge carriers or gaps concentration and can be lightly doped with p or n. This layer produces a high impedance for microwaves when it creates a low capacitance by being reverse-biased (Figure 2.13a). When forward biased (Figure 2.13b) the internal resistance is as low as that of a diode with junctions p and n, changing it to a low impedance [28].

This effect of quickly reducing or increasing the impedance of a channel is what makes

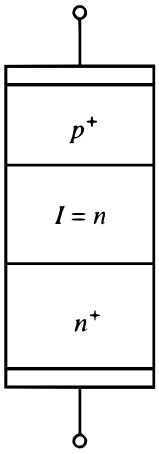

Figure 2.12 – Simplified scheme of constructing a PIN-type diode with the dopings p and n and between them the intrinsic region I. Source: Ludwig e Bogdanov[4]

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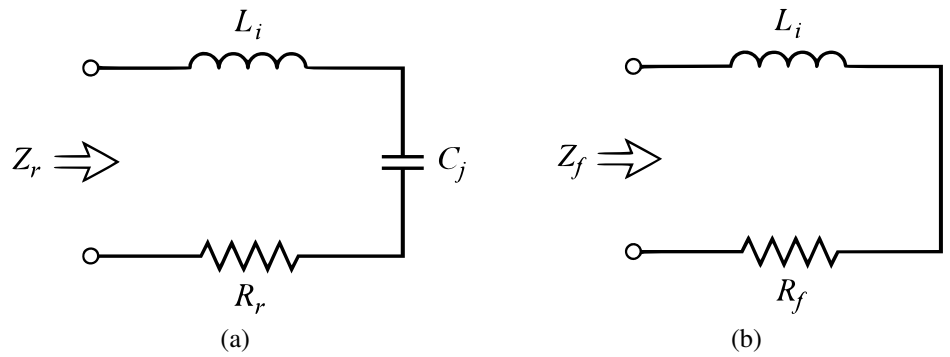


Figure 2.13 – (a) Reverse-biased PIN diode. (b)Directly polarized PIN diode. Source: Pozar[5]

the PIN diode a good switching element, which can also be seen in Figure 2.14.

The PIN diode curve (Figure 2.14) shows the variation of the voltage across the diode for different currents. The reverse bias voltage, V_{REV}, must be high enough so that the RF signal excursion does not cause the diode to reach the breakdown voltage V_B, causing too much reverse current to flow. For forward bias, the forward voltage V_F must be reached. So the diode will have a lower internal impedance for controlling the RF signal [6].

The behavior of the PIN diode is different for low and high frequencies. At low frequencies, below $10\,\text{MHz}$, the transit time of electrons in the i shell is very long. On the other hand, at high frequencies above $1\,\text{GHz}$, the period of the RF signal is much smaller than the time of the minority carriers of the intrinsic region, which allows it to operate in OFF (inversely polarized) and in ON (directly polarized) [6].

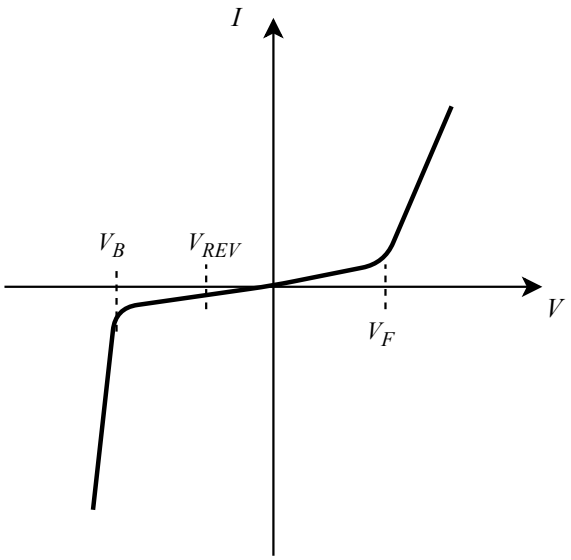


Figure 2.14 – Example curve $V \times I$ characteristic of PIN Diode, showing V_F as the forward voltage, V_{REV} as reverse voltage, and V_B as the breakdown voltage. Source: Adapted from Microsemi Corporation[6].

2.3.1 Switching Speed

Switching speed is essential for transceiver applications. This velocity is the channel formation and breakdown time in the diode when forward and reverse biased. This time is also related to the breakdown voltage $V_B = E_m W$, where E_m is the electrical breakdown field for the diode material and W the width of the [28] channel.

The switching speed is lower for channel extinction, as it is necessary for the loads stored at the boundary of the interstice region to cross it. The minimum time for this switching is approximate:

$$\tau_m = \frac{W}{v_s}. \tag{2.21}$$

For PIN diodes, the switching speed (v_s) is around tens of nanoseconds, and for GaAs PIN diodes, this number reaches 2 ns [28].

2.3.2 Power Handling

The maximum power received by the diode can be described taking into account the peak-to-peak voltage being the same as the breakdown voltage [28]g. It can be roughly expressed as

$$P_m = \frac{V_{RMS}^2}{4Z_0}. \tag{2.22}$$

There is also a relationship between the maximum power that the diode supports and the switching speed. According to Yngvesson[28], for a typical impedance of $Z_0 = 50\,\Omega$ one has

$$\tau_m = \frac{\sqrt{P_m W}}{25}[\text{ns}], \tag{2.23}$$

thus, the greater the power supported by the diode, the longer the channel formation time.

2.4 FIELD EFFECT TRANSISTOR

This section have been extracted from the article [9]. The basics of an RF switch imply a two-state component – ON/OFF state – acting as a control item. In an RF FET switch, the purpose is to control the microwave signal at its terminals, choosing to let signal pass or block it, using field-effect transistors. These FETs may control the signal by changing its internal series resistance (drain-to-source resistance – R_{DS}), applying (or not) just a little amount of power. These aspects create a channel with low or high resistance [8].

First, the FETs, used here as control elements, are electronic components that changing the voltage at the gate, it also changes the channel conductivity, shifting from OFF state to ON state. In these circumstances, there is no – or a small – consumption of current. That implies in a better efficiency compared to a BJT, or even a diode, when the transistor is acting as an on/off key [29].

The basics of the operation of the FET say that its terminals are placed over a layer (n-type or p-type). If there is a potential difference at the gate and the source, the depletion layer turns smaller, and the channel is created, connecting the drain and the source by a low resistance in between them, the R_{DS}. If there is no voltage or it is reversely biased, the depletion area becomes bigger and the channel is pinched off elevating the resistance, and also creating a capacitance, C_{DS} that blocks signals of small frequencies [30]. It all can be seen in Figure 2.15.

Next, FETs are more commonly used in amplifiers and correlated systems, but they are also used in switching systems as control elements. Its high drain-to-source current makes possible a low insertion loss, and when reverse biased, the capacitance helps the insulation [31].

The FET, used as a control element, can be put in series [32]. That way the gate controls whether the port is transmitting or blocking the signal in a direct logical manner [8]. If directly biased, the current may flow throw the transistor so the signal can arrive at the port – ON state. If reversely biased, the current is blocked at the transistor so the signal will not

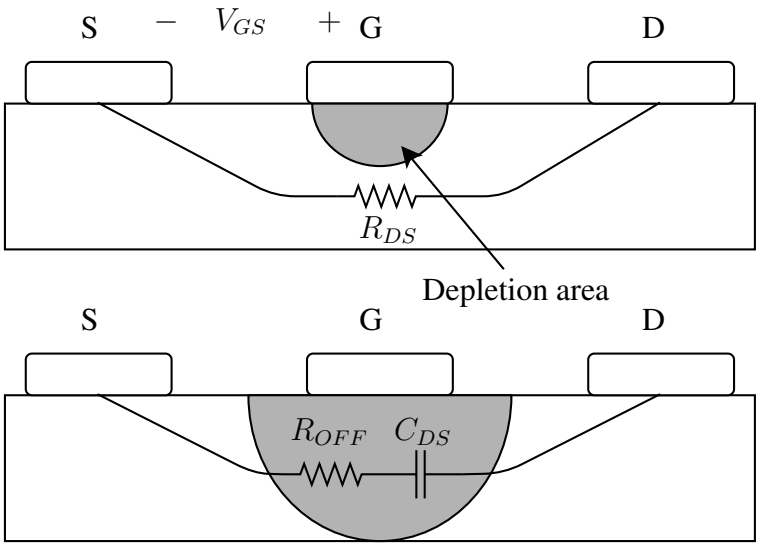


Figure 2.15 – Simplified schematic of a field-effect transistor. At the top, the series resistance between the drain and source, R_{DS}, occurs when there is a potential difference at the gate and the source, V_{GS}. This voltage reduces the depletion area permitting R_{DS} to be low – ON state. At the bottom, the gate and source terminals are at reverse-biasing, causing the depletion area to be much bigger, pinching off the channel. This generate a larger drain-to-source resistance, R_{OFF}, and a capacitance C_{DS}. These circumstances do not allow the signal to pass (OFF state) [7][8].

achieve the port – OFF state.

2.5 S-PARAMETER SIMULATION FOR LARGE SIGNALS

The simulation of S parameters for large signals, better known as LSSP, is one of the several types of simulation that ADS has. It is used to calculate S-parameters for non-linear circuits such as power amplifiers and mixers. The LSSP simulation is based on the harmonic balance and their [33] techniques.

Conventional S-parameter simulations consider small signals from linearized circuits. However, by using harmonic balance, which is a simulation of large signals, LSSP takes into account all the effects of non-linearities in the circuit, such as compression [33]. Therefore, the parameters can vary according to the power variation.

The distortions generated by the non-linearities are critical to the circuit's behavior. They can generate gain compression and even spurious frequencies, more specifically harmonics of the fundamental [5] signal.

Just like the *S_Param*[1] simulation, the LSSP is defined as the ratio of the reflected wave B_i to the incident wave A_j.

$$S_{ij} = \left.\frac{B_i}{A_j}\right|_{A_m=0|m\neq \mathrm{j}}. \tag{2.24}$$

The incident and reflected waves can be described respectively as

$$A_j = \frac{V_j + Z_{0j} I_j}{2\sqrt{R_{0j}}}, \tag{2.25a}$$

$$B_i = \frac{V_i + Z_{0i}^{*} I_i}{2\sqrt{R_{0i}}}, \tag{2.25b}$$

where i and j are the port numbers. V_i and V_j are the Fourier coefficients for the voltages at the fundamental frequency of ports i and j. I_i and I_j are the Fourier coefficients for the currents at the fundamental frequency of ports i and j. Z_{0i} and Z_{0j} are the reference impedances of the ports i and j, and R_{0i} and R_{0j} are the real parts of the respective impedances [33].

For an LSSP simulation on a quadrupole, the complex conjugate of the reference impedance on port 2 is used, and a signal with power P_1 specified on port 1 is applied. Then, with the harmonic simulation, currents and voltages on ports 1 and 2 are calculated together with the calculation of the parameters S_{11} and S_{21} [33].

LSSP uses the complex conjugate of the reference impedance on port 1 to calculate S_{12} and S_{22}. A power signal $P_2 = |S_{21}|^2 P_1$ is applied to port two and, using harmonic simulation,

[1] S-parameter simulation of small ADS signals.

the voltages and currents on ports 1 and 2 are calculated [33].

In this type of simulation, there is a need to use at least one *P_Tone* type port since it allows choosing the output power and the fundamental frequency of the signal. In the same way, in *LSSP* it is possible to choose, mainly, a sweep for the frequency or power, as well as the fundamental frequency (and its harmonics) in each port. Despite being a simulation based on harmonic balance, in the LSSP, it is not possible to analyze the noise figure, requiring the inclusion of other simulations that do so (*S_Param* or *HarmonicBalance*[2]).

[2]simulation of harmonic balance of the ADS.

3 METHODS

This chapter will show the process of choosing a switch element, its development, and the action of the part of the lenses.

3.1 CHOOSING A SWITCH

There are some points that must be noted out of the requirements that the switch must-have. These are in Table 3.1.

Table 3.1 – Main system requirements that affect switch choice

RF Power	IL	ISO	RL	Switching time
$+33$ dBm	Low	High	Low	Low

RF power is an important aspect of the switch. It will receive all the performance of the PA (Power Amplifier). The Power amplifier (PA) chosen in the project of Section 2.1.1 expels a power of $+33$ dBm. Therefore, the switch to be used must withstand at least this nominal energy. The IL and ISO should be low and high, respectively, due to the reasons explained in Section 2.1.2.3. In addition, they must have a considerably low cost, as many will be used for the project.

Market search for switches was carried out in the manufacturers that fit the project. It all was done taking into account the requirements in Table 3.1 and the price. The results are in Table 3.2.

Table 3.2 – Ku-band Switches Market search

Model	Via	Manufacture	Freq. [GHz]	IL [dB]	ISO [dB]	RL [dB]	Power CW [dBm]
MA4AGSW4	SP4T	MACOM	50	0,7	41	21	23
TGS2304-SCC	SP4T	TriQuint	20	0,7	32	9,6	23
MA4AGSW8-1	SP4T	MACOM	50	1,5	32	15	23
MA4AGSW2	SP4T	MACOM	50	0,5	47	22	23
MA4SW210	SP2T	MACOM	20	0,5	50	27	33
MASW-002100-1191	SP2T	MACOM	20	0,5	50	27	33

More switches were identified than those shown in Table 3.2, but those that best meet the

project requirements were listed. Despite this, none of the SP4T[1] found fully meet the needs of the project. During the research, many switches found did not reach the CW power[2] of 33 dBm. Only two switches (MA4SW210 and MASW-002100-1191) have such power capability, but it would be costly as they are SP2T models[3] and lead to a possible cascading of more levels. All models with better results are solid-state, and most with reflective topology.

Switches of the MEMS type were researched, but there were no significant answers for it to continue with its use during the project.

Due to the lack of options in the market that meet the project, it was decided that the RF switch would be designed for satellite communication in Ku-band.

3.2 ELEMENTARY SWITCH DESIGN

It is necessary to create an element that will be repeated along the chain for the switch array design. This element's development involves choosing the topology to be used, the number of outputs, the control element (PIN diode, transistor, or both), the circuit-level simulations, the creation of the bias tee, the electromagnetic simulations, and optimization.

3.2.1 Switch topologies

Considering the factors mentioned in Section 2.2 and a Single-pole double-throw (SPDT) switch[4], there are two main topologies in terms of switching, both presented in Sections 2.2.1 and 2.2.2. These models can be used with one or more control elements in series (Figure 3.1a) and in parallel (Figure 3.1b). They can also be combined with each other, generating a hybrid, series-parallel topology (Figure 3.1c).

As the cascading losses of several switches will be large, one must choose the topology in which there will be the smallest IL. Analyzing the equations of Section 2.2, Keysight Technologies[8] and Street[34] it is possible to notice differences in IL and ISO between both topologies.

When analyzing the Equations 2.13 and 2.18, it is observed that the insertion loss with the control component in parallel is smaller than that with the same component in series. In Equation 2.13, for the IL to be low, the R_{on} must be low, and getting this R_{on} in active components is more expensive. As for Equation 2.18, it is only necessary that the capacitance has a low value, C_{OFF}. This low IL is not difficult to achieve with the right geometry, doping,

[1] *single-pole four-throw* switches used to describe a switcher with one input and four outputs.
[2] continuous wave power.
[3] *single-pole double-throw* in English, used to describe a switch with one input and two outputs.
[4] another acronym for a switch with one input and two outputs.

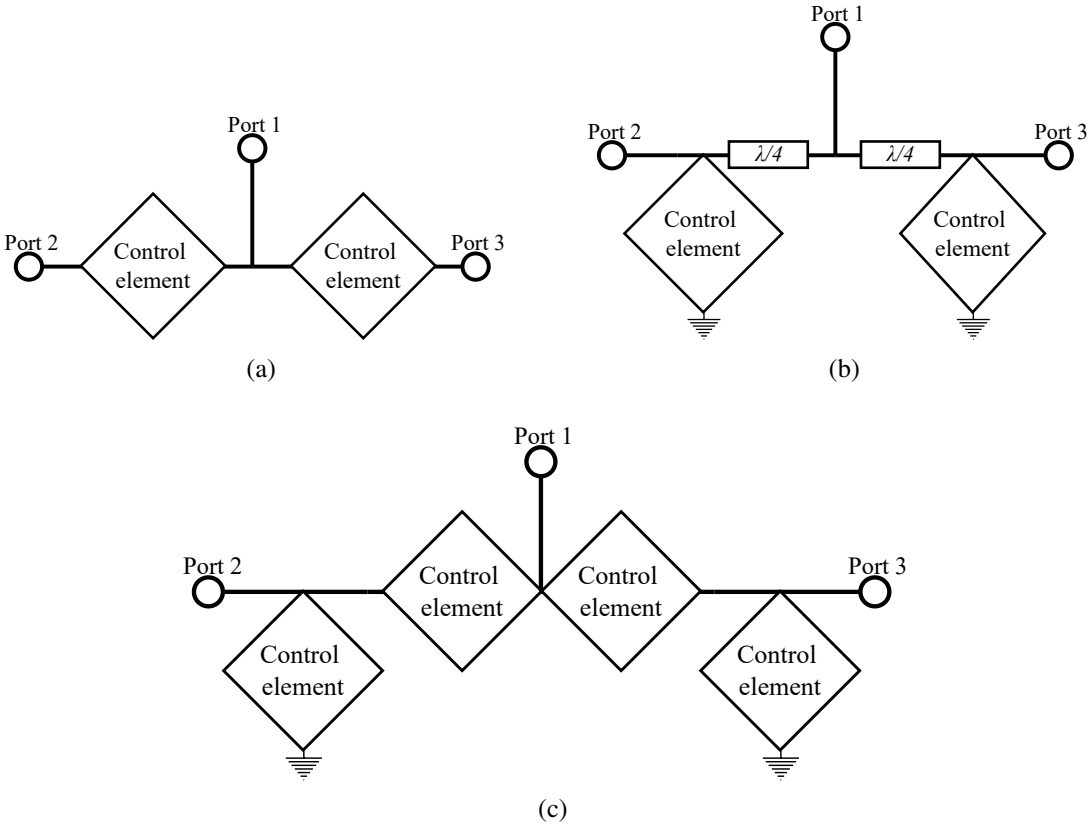


Figure 3.1 – Different topologies showing for different positions of control elements – (a) series, (b) parallel and (c) series-parallel – in an SPDT switch. Source: Own elaboration.

and elements and can even be caused even with a not-so-high R_{OFF}.

Street[34] shows that using elements in parallel in a switch has a lower IL than the same element placed in series or series-parallel designs. It also shows that the higher the bias current, the lower the internal resistance of the control component. For these reasons, the topology chosen was the one with control devices in parallel.

3.2.2 Control Element

Insertion loss will also be considered when choosing the control component as it is such an essential factor. Two other significant issues to consider are vibration resistance and power capability. Vibration resistance, because the final equipment (transceiver and radiating system) will be used in vehicles, and power capacity because $33\,\text{dBm}$ for an RF signal is a significant value, and possibly this incident power value will increase in the subsequent phases of the project.

It was possible to set up a comparison (Table 3.3) with control devices about essential parameters for the project. Through a review of literature and manufacturers' application manuals.

Table 3.3 – Comparison between switches with different control elements. Adapted from Keysight Technologies[8]

	PIN Diode	FET	Hybrid	MEMS
IL	Moderate	High	High	Low
ISO	Good	Good	Good	Good
Switching Time	Fast	Moderate	Moderate	Slow
Incident Power	Moderate	Low	Low	High
Life Cycle	High	High	High	Moderate
Consumption	High	Low	Moderate	Low

MEMS-type devices would be the best choice. Despite the switching time being the longest among the options in the 3.3 table, this period is still low (it is in the range of tens of milliseconds). In addition, companies were contacted for quotations but did not respond to messages. For these reasons, this option was discarded at this project stage.

The following solution is the use of PIN diodes. They support a more significant amount of power, have fast switching, and have a lower IL than the rest. For these comparisons, the PIN diode was chosen as the control device for switching the ports.

3.2.3 Choose the PIN diode

PIN diodes that meet the project need to be seen in Table 3.1 were searched in the manufacturers and sellers catalogs. Unfortunately, despite the high number of diodes on the market, few were found with the necessary specifications. It is also remembered that the required power of $+33\,\text{dBm}$, which is equivalent to $2\,\text{W}$, will have to be supported by this same diode.

The diodes with the best characteristics were found in the manufacturer MACOM and are shown in Table 3.4.

Table 3.4 – Comparison between diodes with different parameters within the design specifications.

Diode	Max Freq. [GHz]	CW Power [W]	Resistance [Ω]	Capacitance [pF]
MA4SPS502	26	10,0	2,4	0,14
MEST2GFC-010-25	40	10,0	2,0	0,04
MA4P161-134	18	2,3	1,5	0,10
MA4P203-134	18	5,0	1,5	0,15
MA4P303-134	18	5,0	1,5	0,15

The diode chosen was the MA4SPS502 [35] because its operating frequency is within the

Ku band, due to the other attributes and the power that can reach up to $10\,\mathrm{W}$ CW ($40\,\mathrm{dBm}$). Its SPICE model and others can be found in its datasheet.

3.2.4 Substrate and fabrication limitations

A substrate that includes these elements is necessary because the switching circuit will be made in a microstrip with Surface mounted components (SMD) components. This substrate affects the *design*, the size of the microstrip track, and consequently its impedance in the circuit.

It is necessary for the project a substrate that has a low electrical permittivity constant so that the tracks are more extensive due to the high frequency that has the reduced electrical lengths. Furthermore, it is also necessary that this substrate has a smaller thickness so that the dielectric losses due to the tangent of losses are minimized. Therefore, the substrate AD250C™from Rogers Corporation[11] was chosen, which is the PTFE/fiberglass base for the entire project.

Table 3.5 – AD250C™main substrate specifications. Source: Rogers Corporation[11]

ε_s	$\tan\delta$	Substrate thickness	cladding
2,52	0,0013	0,508 mm	1/2 oz.(18 μm)

From the choice of substrate, a search was started for printed circuit manufacturers that had the process to work with PTFE. In Brazil, only Micropress was found that works with AD250C™.

Table 3.6 – Micropress key technical capabilities that affect RF switch design at minimum values. Source: Micropress[12].

Microstrip width	Insulation between conductors	hole diameter	island width
4 mil(0,102 mm)	4 mil(0,102 mm)	6 mil(0,152 mm)	5 mil(0,127 mm)

The development of the switch circuit depends on the technical capabilities of Micropress[12]. The limitations that most affect the design are the width and isolation of tracks, along with the drilling and size of islands (Table 3.6). Circuit design cannot be outside of these Micropress manufacturing limits.

3.2.5 Circuit-level simulations

Tests were done to achieve a low IL and a high ISO to arrive at the best possible switch. The tests consisted of small-signal S-parameter simulations made in the ADS program and

not the LSSP, as it is just verification, not representing the final circuit. We used the package *TLines-Ideal* from the program itself – which is used to simulate ideal transmission lines – together with the model *PinDiodeModel* – which is a tool to describe PIN diode models - - with the data from the *datasheet* of the MA4SPS502 diode.

First, the test was performed with a diode in parallel (Figure 3.2a) and later with two diodes in parallel (Figure 3.2b). Ideal elements (*DC_Block* and *DC_Feed*) were used to polarize the diodes and separate the RF and Direct current (DC) signals.

In the simulation, the diodes are separated by a transmission line. It is possible to adjust the desired frequency for the operation of the switch with modifications in this transmission lines [8], increasing the ISO and reducing the IL and RL.

These better results are due to the characteristic of the lines of $\lambda/4$ (Appendix A), which has the effect of impedance inversion [34]. The $\lambda/4$ length of the Transmission line (TL) was set to an impedance of $50\,\Omega$ and a center frequency of 13.1 GHz defined by a geometric mean,

$$f_c = \sqrt{f_1 f_2}, \tag{3.1}$$

where f_1 and f_2 are the Ku-band threshold frequencies (11.7 GHz and 14.5 GHz).

The simulations were configured for communication between ports 1 and 2. The main parameters were shown: S_{11} for RL, S_{21} for IL and S_{31} for ISO. Figure 3.3 shows the simulation for SPDT with one diode per channel and Figure 3.4 two diodes per channel.

The best results achieved consisted of the circuit with two diodes in parallel per output. As a result, the isolation was increased, and the insertion loss and the return loss were reduced by adding a diode and an TL of $\lambda/4$ per channel compared to the circuit of only one parallel diode per channel.

It is essential to report an overload warning on the diodes that were forward biased. This warning was due to the excess current that extrapolated the dissipated power of the diodes. The warning is not a problem as it is still a verification test and will not be part of the final design.

Later in the dissertation, a resistor will be included in the components that bias the diode to limit the current and, consequently, the power dissipated by the diodes. It is worth noting that the dissipated power warning is 2 W and that the maximum incident current is 600mA.

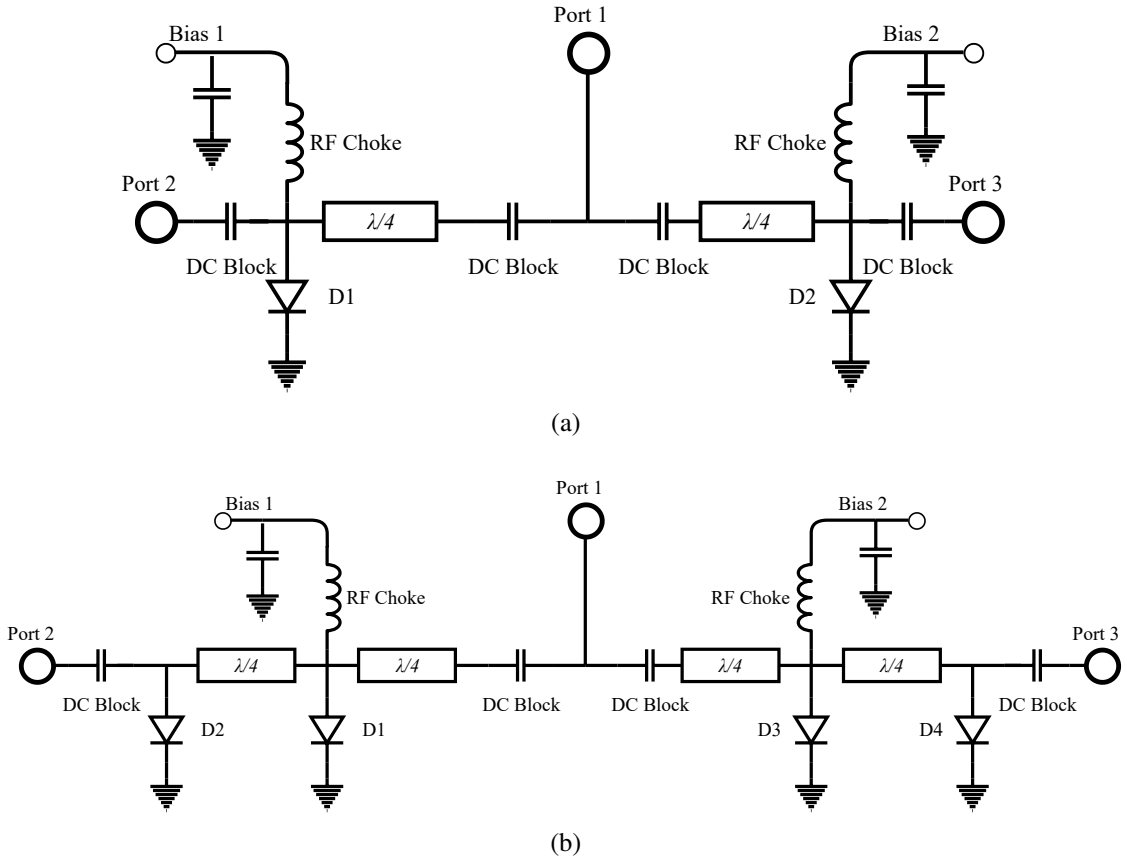


Figure 3.2 – Diagram of an SPDT switching circuit with (a) one diode and parallel and (b) two diodes in parallel, separated by a transmission line of $\lambda/4$. Source: Own elaboration.

3.2.6 SPDT circuit development

the design of the switching circuit was started with the knowledge of the topology and the number of diodes. For the microstrip-level circuit on a substrate, *MLIN* was used, and the other packages of *TLines-Microstrip* that have this function and LSSP between 10.5 and 15.5 GHz.

Substrate losses are taken into account using this package. The SPDT circuit was simulated with the ideal biasing to optimize the distance of $\lambda/4$ between the diodes and thus improve the isolation insertion loss. The schematics created are in Appendix B.3

The circuit was made based on the chosen substrate information explained earlier in Table 3.5. Several types of junctions were tested between the three channels, and the one that obtained the best result (in terms of IL and ISO) was the junction in the form of "T" (channels 2 and 3 orthogonal to the channel 1).

We also tested various track widths and observed that there is a trade-off. Wider microstrip tracks have a better IL and worse ISO, and thinner tracks have better ISO and worse IL. A width of approximately 0.580 mm with an impedance of approximately $80\,\Omega$ was then chosen. The schematic of the assembled circuit is in Appendix B.3.

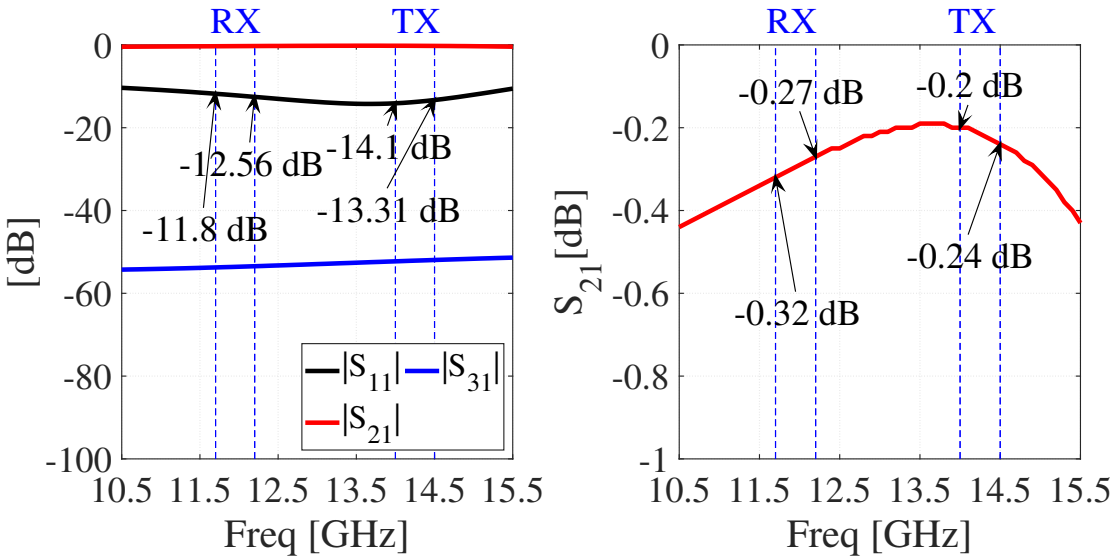


Figure 3.3 – Simulation results of an SPDT with one diode per channel showing on the left S_{11} as RL, S_{21} as IL, and S_{31} as ISO, and on the right in detail the insertion loss. Source: Own elaboration.

After optimizing the schematic, the circuit was transferred to the ADS *Layout* environment (Figure 3.5). There, electromagnetic simulations are carried out based on moments that have results more in line with reality. This electromagnetic circuit has also been optimized.

Spaces and *pads* correlated to the 0204 sizes of resistors and capacitors for the SMD components were left. For the diodes, the *pads* and the spacing between them, the specifications of the *datasheet* were used. This circuit still used components of biasing and separation of ideal signals.

3.2.6.1 Bias Circuit

The biasing of the diodes is another crucial part of the elementary switch. There must be a continuous potential difference between their terminals as they are active components.

Even more important is that the direct current generated by this voltage does not reach the RF ports and that the RF power is not diverted to the source that generates the direct voltage. This miss power could permanently damage the transceiver and pointing control.

For this, a biasing circuit known as bias tee was created (Figure 3.6) that replaces the ideal components *DC_Block* and *DC_Feed*. For this, radial stubs were used[5] microstrip with small widths (at the manufacturing limit) and capacitors.

The choice of the capacitor was based on impedance so that it blocks the DC signal and lets the RF signal through. The impedance of a capacitor can be described as

[5] *radial stub* in English

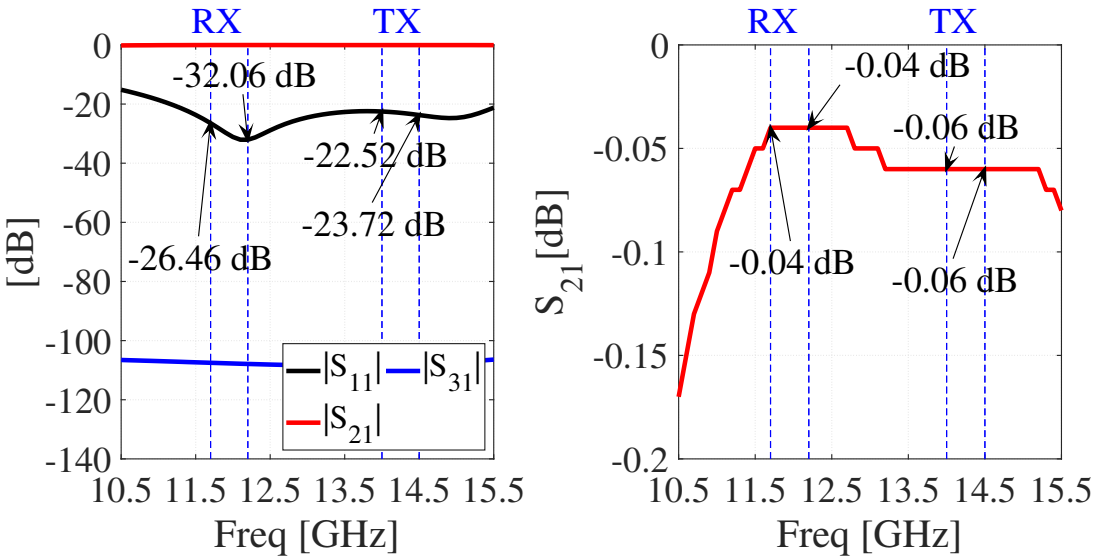


Figure 3.4 – Simulation results of an SPDT with two diodes per channel showing on the left S_{11} as RL, S_{21} as IL and S_{31} as ISO and on the right in detail the insertion loss. Source: Own elaboration.

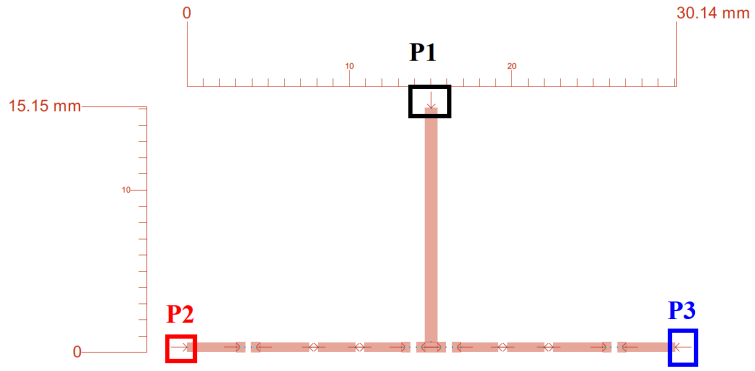


Figure 3.5 – SPDT switching circuit on microstrip in the *Layout* environment showing the channel of port 1 in the center (vertically) and the channels of ports 2 and 3 (in the horizontal), respectively, on the left and right. Source: Own elaboration.

$$Z_{cap} = -\frac{\mathrm{j}}{2\pi f C}, \tag{3.2}$$

where C is its capacitance, and f is the lowest frequency of the Ku band. Z_{cap} should be as small as possible for this frequency, allowing the passage of any spectrum within the Ku band,

$$C = -\frac{\mathrm{j}}{2\pi f Z_{cap}}. \tag{3.3}$$

Z_{cap} is stipulated to be less than $-0.005\mathrm{j}\,\Omega$. Thus, the capacitance C must be greater than $2\,\mathrm{nF}$. A capacitance of $10\,\mathrm{nF}$ was chosen for a safety margin.

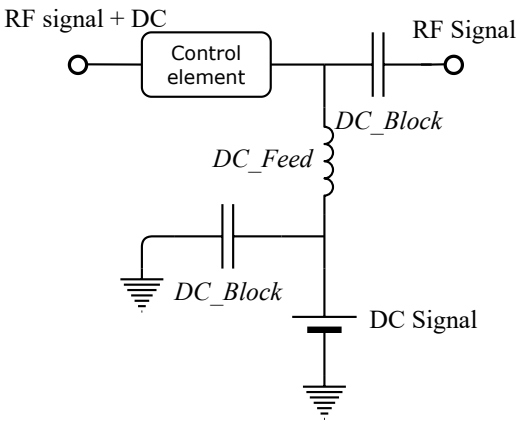


Figure 3.6 – Diagram with an example of a bias tee where discrete elements separate the RF and DC signal. Source: Own elaboration.

The next step was to develop the rest of the bias circuit: radial stub and transmission line of $\lambda/4$ (Appendix B.1). For this, the *website* Microstrip...[36] was used, which obtained satisfactory approximations for the equations described by Atwater[37] for radial stubs that work as capacitors for high frequencies.

The $\lambda/4$ lines need to have a high impedance at high frequencies so that the RF signal does not pass. This can be achieved with minimal microstrip widths. The smallest width available for this copper substrate thickness is $0.102\dot{m}m$.

To solve the problem of the high currents of the diodes, we used a circuit with a resistor of $50\,\Omega$ in series for each diode (Appendix B.2) in order to reduce the power dissipated by the PIN diode. A capacitor was also placed to make the RF signal reach the ground and $\lambda/4$ lines so that this same RF signal does not reach the resistor. They were tested with radial stumps in place of the capacitor, but the best response was with an SMD device.

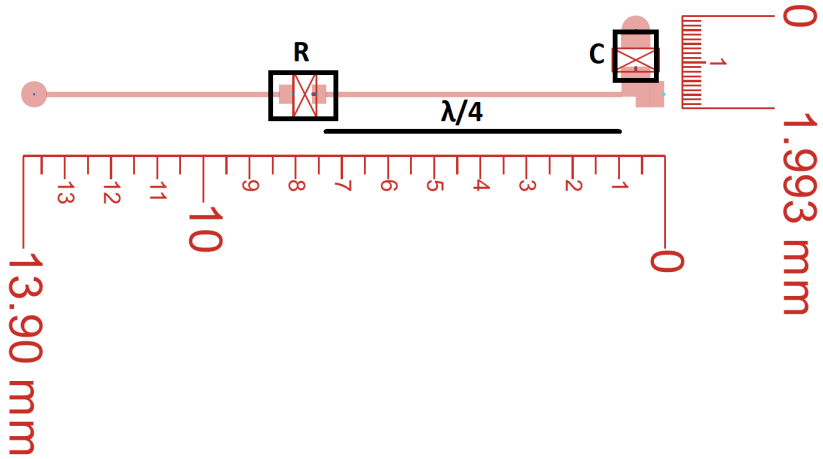


Figure 3.7 – PIN diode bias circuit in the ADS *Layout* environment. Diode current reduction circuit with a capacitor C of $10\,nF$ parallel with resistor R of $50\,\Omega$. Source: Own elaboration.

After simulations and optimizations, the circuit was transferred to the layout environ-

ment, and again, it was simulated and optimized so that the RF signal lost to the DC source was minimal, even with the ideal bias circuits.

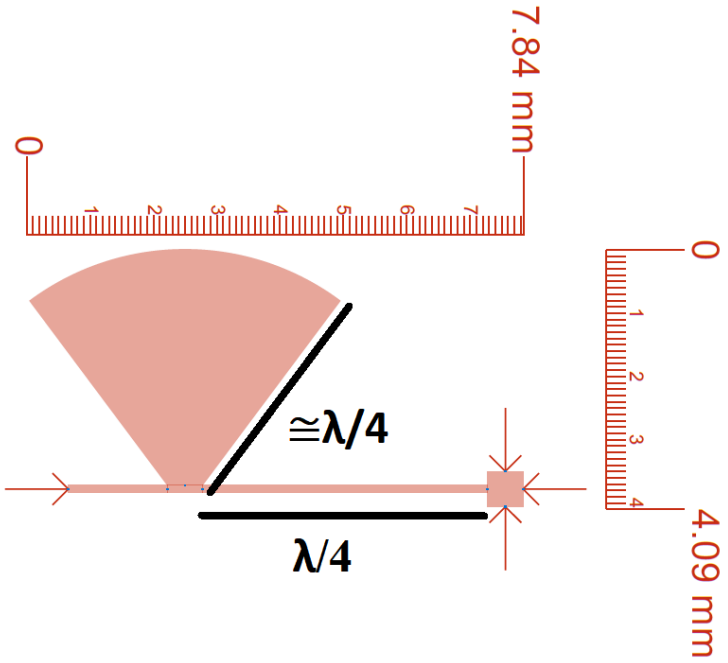


Figure 3.8 – PIN diode bias circuit in the ADS *Layout* environment. Bias tee with radial *stub* radius of $\lambda/4$ and access line of also $\lambda/4$ and 0.102 mm. Source: Own elaboration.

3.2.6.2 SP2T full circuit

Now, with the bias circuits completed, it is possible to unite the designed circuits and simulate the operation of the RF SPDT switch. The circuit was assembled and optimized in the ADS *Schematic* environment (Appendix B.4). The circuit was set up so that the tracks parallel to each other were as far away as possible, thus minimizing the coupling effect between them.

In the first figure in Appendix B.4 is the SPDT switching circuit on microstrip in the *Schematic* environment, showing the channel of port 1 in the center, and the channels of port 2 and 3, respectively, on the left and the right.

Afterward, the circuit was transferred to the *Layout* environment and simulated with the method of moments and also optimized (Appendix B.4). For these optimizations, it was necessary to be very careful with the limits of the variables used in the bias tee. The radial stump tracks could be overlapped, making it possible to de-characterize the RF switch. In the second figure of the same annex is the SPDT switching circuit in microstrip in the *Layout* environment showing the measurements of the switch and the switch with access lines of 5 mm and characteristic impedance of $50\,\Omega$ in the ports 2 and 3.

The final circuit of the SP2T switch (Figure 3.9) has dimensions of approximately 40 mm $\times$ 30 mm.

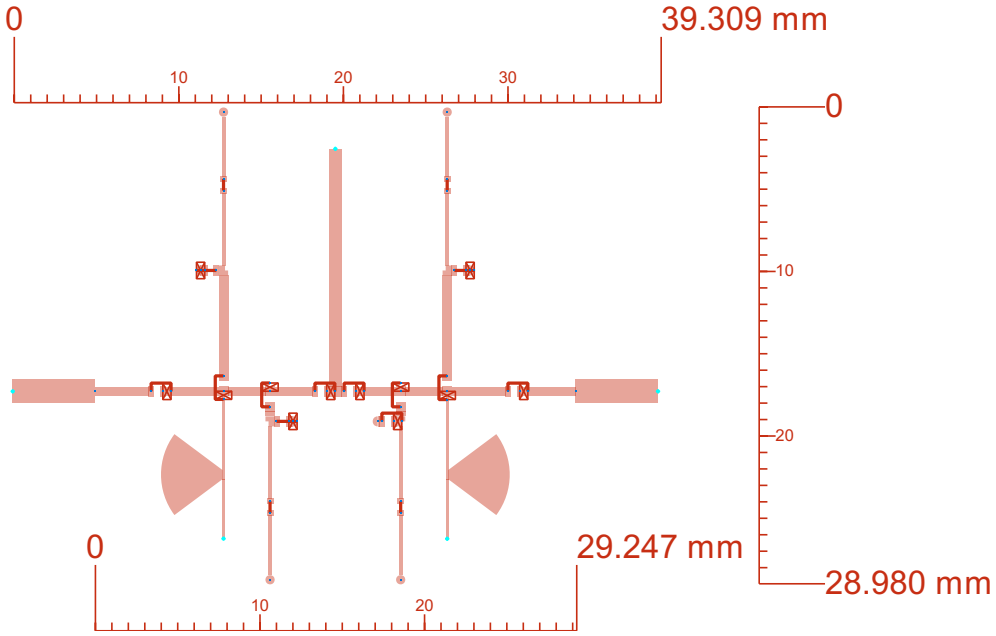


Figure 3.9 – SPDT switching circuit on microstrip in the *Layout* environment showing the measurements of the switch and the switch + access lines of 5m̀m and characteristic impedance of $50\,\Omega$ on ports 2 and 3. Source: Own elaboration.

This scale is reasonably good for a circuit made up of dozens of these same elements.

3.2.7 Development of the SP4T circuit

From the development of the SPDT circuit (Section 3.2.6) it was possible to start the circuit of a switch with more ports. Despite being a more complex design, the SP4T will make creating an array of switches easier.

A switch *Single-pole Four-throw* consists of a port common to four other ports through which the signal must pass when activated. As with SPDT, with the use of two diodes in parallel per channel, this new switch changes the impedance of the ports to allow communication or block the signal.

Following the same methods shown for the development of SPDT (Section 3.2.6). The microstrip circuit was simulated in ADS using the tools available in the *TLines-Microstrip* package and later taken to the *Layout* environment. The substrate used was AD250C™, the same used in SPDT (Section 3.2.4). For SP4T LSSPs were made between 9ĠHz and 17ĠHz.

In the SP4T switch circuit, a characteristic impedance of $50\,\Omega$ was chosen, corresponding to a width of 1.41 mm. For the discrete SMD components (resistors, capacitors, and diodes)

pads of dimension in the 0204 standards, very used commercially, were used. The PIN diodes used are still from the MACOM model, MA4SPS502, as they have to meet the exact previous specifications.

3.2.7.1 SP4T bias circuit

Another bias tee design was created for better insertion loss response. In this new 4-channel switch, a bias circuit with two radial stubs was used.

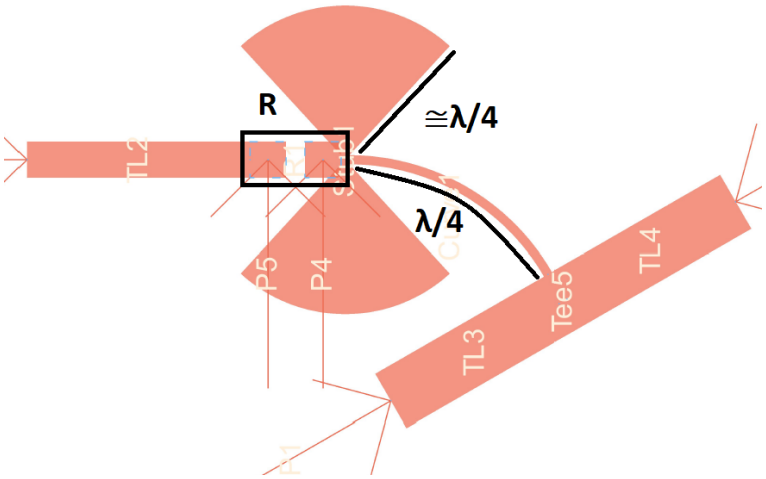


Figure 3.10 – Bias circuit of the PIN diodes in the *Layout* environment of the ADS. Bias tee with double radial stub of radius approximately $\lambda/4$ and access line of also $\lambda/4$ and 0.160 mm. Source: Own elaboration.

In this way, only a single bias circuit is needed for the pair of diodes in parallel to each channel (Figure 3.10). This makes it possible to reduce the number of components for the bias tee (from two resistors to one and from two capacitors to none), which also decreases the total value of each unit produced.

3.2.7.2 SP4T full circuit

With the bias circuit established, four different versions of the switch from 1 to 4 were formulated to verify which one has better IL, RL, and isolation performance. The version with the best performance was the SP4T version 2.0 circuit, so it was chosen for the matrix and presented next. The other versions are available in Appendix C.

SP4T v2.0 is designed with four channels and one main channel, common to all others. Each channel has two PIN diodes in parallel, and a bias tee was created earlier (Section 3.2.7.1).

During the development of this switch, it was noticed that the smaller junctions between the channels, the better the performance. The smaller the area of metal that joins the tracks

of the channels, the better the communication between them, which leads to better insertion loss, better return loss, and better isolation between channels.

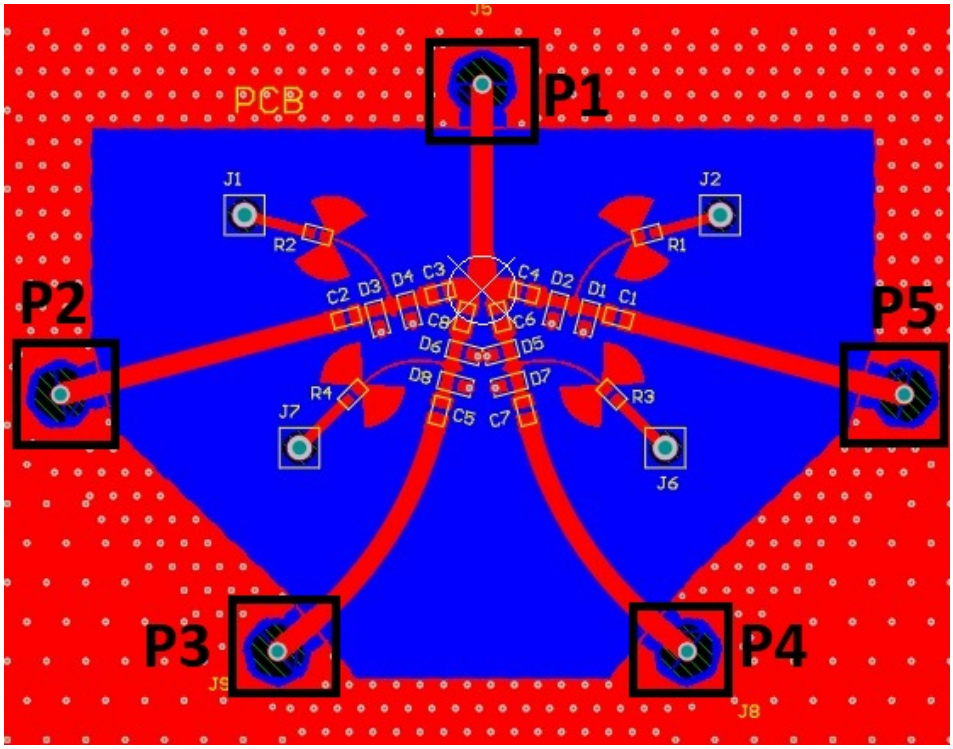


Figure 3.11 – Switching circuit SP4T version 2.0 in complete microstrip in the *Layout* environment showing switch, ports (P1 as main and P2 to P5 for the other channels), and ground (in red) with *through hole* paths. Source: Own elaboration.

At first, an LSSP simulation was made of the different elements simulated by the method of moments at the schematic level. Later, they were merged into the same structure for the electromagnetic simulation. The final result was optimized after the first simulations. The ports are represented by the abbreviations P1, P2, P3, P4, and P5, in black in Figure 3.11. In addition, a ground plane (in red) has been included on the circuit board to minimize interference and ways to connect the ground planes and keep them equipotential.

The SP4T (Figure 3.11) has a size of 21 mm $\times$ 31 mm. This extension achieved with the SP4T circuit is already smaller (and therefore better) than the area occupied by the SPDT. It also uses fewer components in proportion to the number of channels. The evolution achieved with the SP4T switch was significant for the project.

3.3 SP16T MATRIX

The matrix of microwave switches, MSM, is the cascading of switching elements in series to increase the number of outputs. It was built with the best performing switching

element, SP4T v2.0. The SP4T (Figure 3.11) is 21 mm $\times$ 31 mm. This extension achieved with the SP4T circuit is already smaller (and therefore better) than the area occupied by the SPDT. It also uses fewer components in proportion to the number of channels. The evolution achieved with the SP4T switch (in terms of reliability) was significant for the MSM project.

The switch array is designed on the AD250C™substrate with the best SP4T switch version. It uses five SP4Ts v2.0 devices, cascaded in two levels providing a 1 to 16 matrix (SP16T).

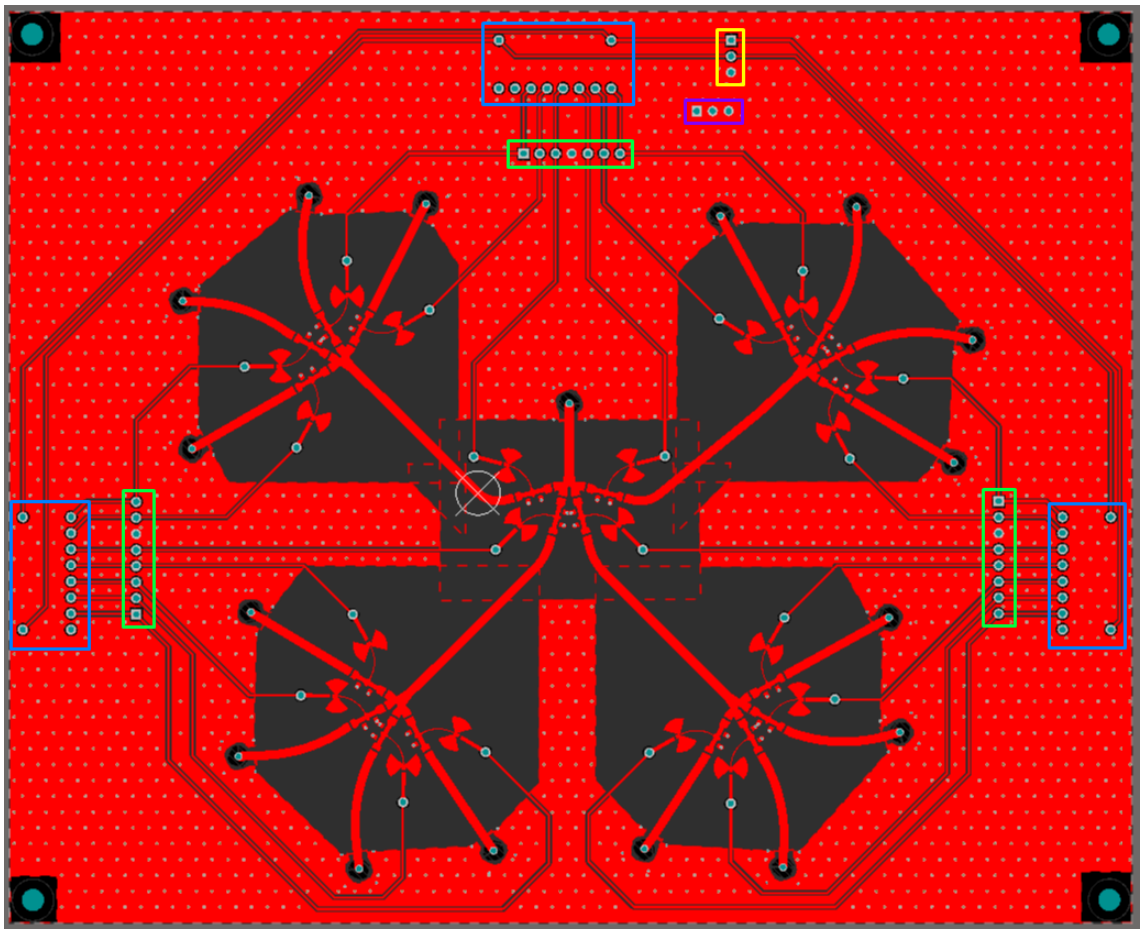


Figure 3.12 – SP16T matrix is 5 SP4T v2.0 switches cascaded into two levels ready for manufacturing. The thinnest tracks are control signals taken from switches to pins (in green) and paths destined for control devices (*DIP switches* in blue). In purple are pins for the GND, and in yellow are the pins for $+1$ V,-4 V, and GND. Source: Own elaboration.

For the MSM tests, a control device was needed to replace, for the time being, the control that the Field Programmable Gate Array (FPGA) will do. A DIP switch TDS08 from APEM inc.[38] with 8 selector switches and 3 positions each (+,0,–) was chosen. Control is done by applying a voltage of -4 V (ON-state of the channel), and $+1$ V (OFF-state).

Pins were also placed on the MSM board (in green in Figure 3.12) so that, if necessary, the workgroup responsible for SDR can connect them to the FPGA and thus carry out more control tests. A ground plane was placed at the top (in red) to reduce coupling between

RF tracks. trough hole paths were placed between the two ground planes to maintain the same potential throughout the plate. The spacing between pathways was specified to be at a distance less than $\lambda_g/8$ so that resonances would not be created.

Access tracks of 20 mm with different curvatures were allocated at the main switch's outputs that connect all the others. This placement was done so that the other switches could be far enough away from each other and thus cause and suffer minimal interference from the other devices. These tracks were also placed on the 16 output ports to perform tests with Subminiature push-on (SMP) type connectors and adapters.

3.4 RF FET SWITCH

All this development have been made previously in the article [9]. The developed FET switch was designed due to problems in testing the PIN diode switches. There were some problems with what was think to be the biasing. Due to this, it have been thought in a simpler designer with a smaller band, and less power handling.

the FET switch was designed in microstrip technology to operates between 11.7 GHz and 12.2 GHz for the receiving band, with four ports and a lower noise figure. There are few devices with these configurations (with so many ports, that it is intended for these frequencies and with low noise) in the current market. With that said, the designed switch is very near to the state-of-the-art of an RF solid-state commutator.

Having in mind that the designed RF FET switch is part of the main project with transceiver, radiating system, there are previous specifications that need to be taken into consideration. The whole system is supposed to function from 11.7 GHz to 12.2 GHz. It is important to have a low insertion loss, due to transmitted and received signals from a geostationary satellite, once that power is the most important and expensive parameter in RF systems. It also needs high isolation to keep a highly collimated beam and as many ports as possible. When using transistors, the power consumption gets lower and the noise generated is also lower compared to the PIN diode. Different from [39], the power handling at this conceptual design is not important.

From previous works ([39], [8], [7], [40]) it is known that designs with control devices in parallel have better results on isolation and insertion loss. That way, the RF FET switch is designed with four ports and transistors in parallel, one for each terminal. It was decided to develop this circuit with microstrip technology on a printed circuit board. This simplifies manufacture and may enable a reduction in scale costs in the future.

The substrate chosen was the RO4350B™[13] in Table 3.7. It is made of PTFE and can be manufactured with the same process of FR-4, which makes it easy and cheaper to be

fabricated. In addition, it has low loss and low dielectric tolerance.

Table 3.7 – RO4350B™substrate main specifications [13].

ϵ_s	$\tan\delta$	Thickness	Cladding
3.66	0.0037	20 mil(0.508 mm)	1/2 oz.(18 μm)

The bias circuit is also an important part. It needs to provide insulation for both the control system and the RF circuit. Since it is desirable a small RF switch, the bias has to be small and may not interfere with other parts of the circuit. The bias tee designed uses a quarter-wavelength microstrip working as an inductor to create an impedance miss-match, and a radial stub as a broadband capacitor to avoid spikes from the DC control system.

For the SP4T, each branch is designed to have the quarter-wavelength microstrip from the junction to the FET, and the bias tee to control of the ports the switch (Figure 3.13).

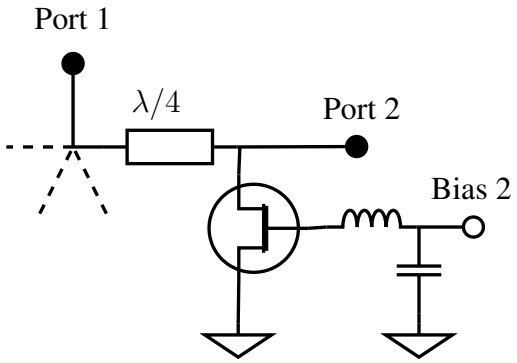


Figure 3.13 – Simplified schematic of the SP4T FET switch. It is shown the main port and one branch with the quarter-wavelength transmission line for the matching, the transistor used as control element, the decoupling capacitor to prevent spikes at the port, and the RF choke – represented as an inductor – to isolate the bias circuit from the RF circuit. Source: Nascimento, Sousa e Rondineau[9].

The transistor is the main part of this system, and its choice impact many aspects of the design: frequency of operation, impedance matching, insertion loss, isolation, power handling, noise figure. After market research, it was found the CE3512K2 [14], from CEL (Table 3.8). It is a p-type JFET with a low noise figure and designed for Ku-band.

Table 3.8 – CEL transistor, CE3512K2 main typical specifications [14]. Source: Nascimento, Sousa e Rondineau[9].

V_{DS}	I_D	V_{GS}	Noise Figure	Freq.	Technology
4 V	10 mA	-3 V	0.3 dB	12 GHz	GaAs

The transistor packaging is the Micro-X plastic package, where there are 4 pads – two for the source, one for the drain, and one for the gate – in a cross shape. The two source pads oppose each other, and the drain and gate pads oppose themselves. Taking advantage of that, the source pads were grounded utilizing it as a common-source design, connecting the drain right after the quarter-wavelength microstrip. Various metallic vias were made to better connect the ground plane and the source pads (Figura 3.14).

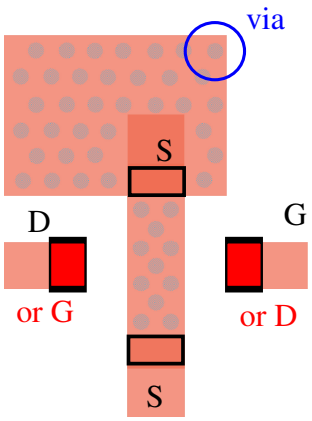


Figure 3.14 – Upper view of the microstrip pads designed to receive the CE3512K2 transistor. Each pad designation is marked (in black or red) for the source, drain and gate. When necessary, it is possible interchange the side of the gate and the drain, and vice versa. Several metallic vias through interconnected (circled in blue) between the ground plane below and the surface microstrip were made for a better grounding of the source pads. Source: Nascimento, Sousa e Rondineau[9].

The main design of the RF SP4T FET switch incorporates all of what was previously stated – bias circuit, transistor, topology, pads, etc. These aspects were applied and combined in a microstrip structure with 4 branches and four bias points to select which port is ON or OFF (Figure 3.15). This final design is ready for fabrication and its size is only 27 mm$\times$37 mm. It is really small, making it easier to relocate or cascade if more ports are needed, and also cheaper when scaling.

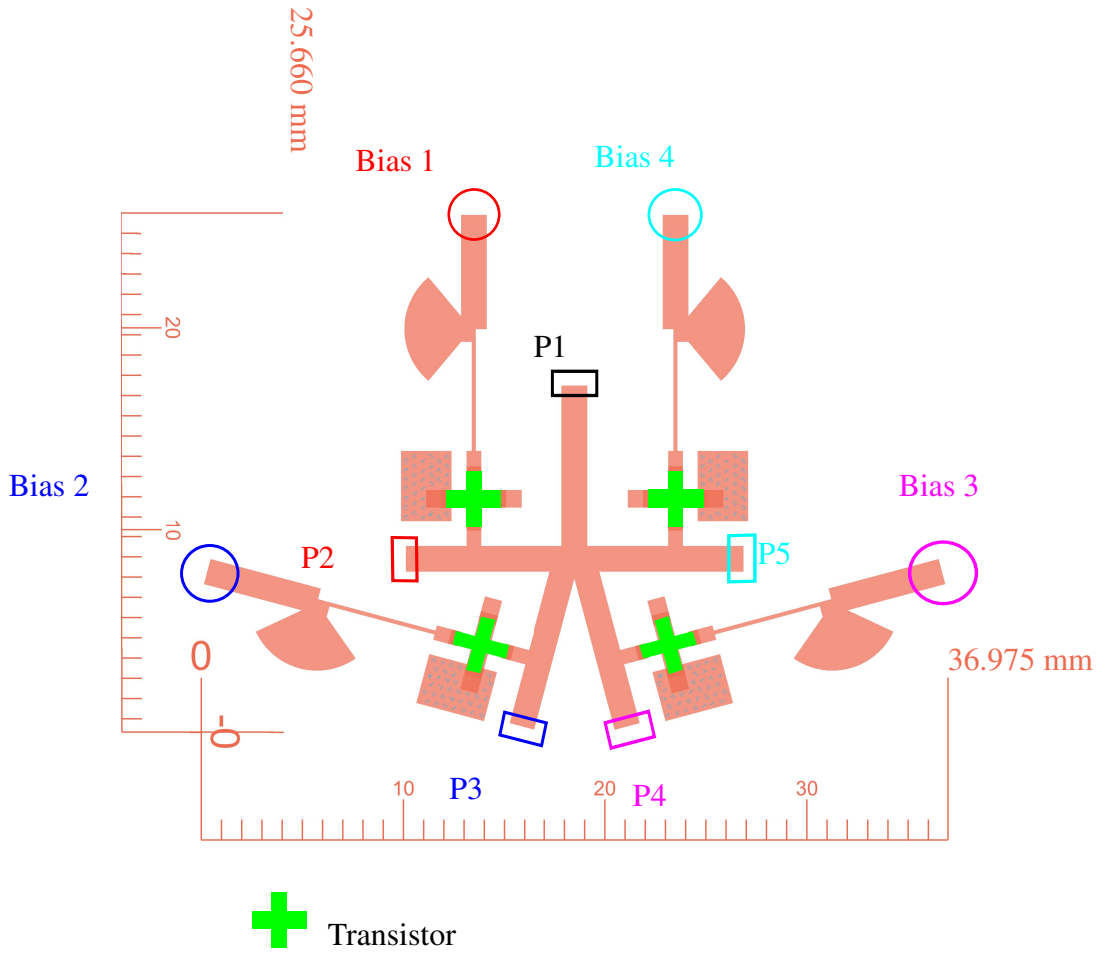


Figure 3.15 – RF SP4T (single-pole four-throw) FET switch using transistors CEL/CE3512K2 in parallel. In this design, it is applied the quarter-wavelength microstrip line before the JFET, the bias tee with radial stub, and the JFET Source pads grounded by vias. The maximum dimensions for this switch are approximately 26 mm×37 mm. Source: Nascimento, Sousa e Rondineau[9].

3.5 ROTMAN LENS DEVELOPMENT

A lens was developed to test and verify the operation of the beam steering system at the simulation level. The design of this microwave lens operates between 11.7 GHz and 12.2 GHz (Ku-band), which, together with an RF switch, is part of a beamformer for a mobile satellite communication system. Unlike other beamformers, this lens has a wide bandwidth due to its geometry and true-time delay. Another interesting point is that, if well designed, it is almost sure that the entrance angle of the port translates into the pointing angle, making it reliable and robust to minor manufacturing errors.

This circuit was developed to have seven different pointing angles (between $\pm 30^\circ$ with intervals of 10°), to meet a linear arrangement of 8 elements, and to be manufactured in microstrip on a printed circuit board, allowing a large-scale production.

For the lens design, an RF circuit development software was used with libraries, and the

equations involving its geometry [26]. An FR-4 substrate was chosen with the thickness and data in Table 3.9

Table 3.9 – Main FR-4 substrate specifications.

ϵ_s	Thickness	Cladding
4.5	20 mil(0.508 mm)	1/2 oz.(18 μm)

The primary data of a lens were provided to the simulator and were the desired center frequency of downlink of the Ku band (11.95 GHz), the number of beams, and the maximum angle (Table 3.10). With these parameters, a Rotman lens was generated (Figure 3.16)

Table 3.10 – Rotman lens design key specs.

f_0	Z_0	ϕ_{max}	M	N	Length	Width
11.95 GHz	80 Ω	30°	7	8	81.34 mm	66.21 mm

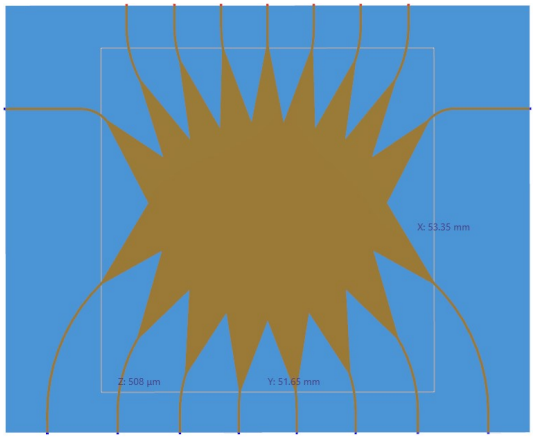


Figure 3.16 – Rotman lens in development software shows seven beam ports (top), which allow for seven different aiming angles. The bottom eight outputs are shown. Its dimensions are approximately 81.34m̈m× 66.23m̈m.

For the generated lens, the software also pre-analyzes the planar geometry operation and creates the graphs of the arrangement factor for each direction (Figure 3.17).

Later, this lens was exported to another radio frequency electromagnetic simulation software (Figure 3.18). The simulation performed was one of the S-parameters for the 15 ports. This simulation checks the transmitted and received powers between the ports and their respective delays (phases). After the successful simulation, a file *.s15p* was generated with all parameters between the 15 ports, and this file was analyzed in Matlab.

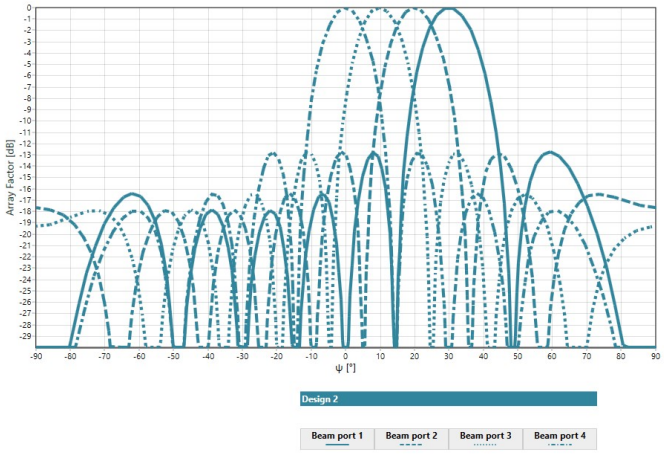


Figure 3.17 – Analytically calculated arrangement factor of the 7x8 lens in the development software. The beam angles are in Table 3.11 As it is symmetric, the first four beams are shown.

Table 3.11 – Maximum beamformer aiming directions for ports 1 to 4, analytically calculated by software.

Port 1	Port 2	Port 3	Port 4
30.08°	19.85°	9.86°	0.00°

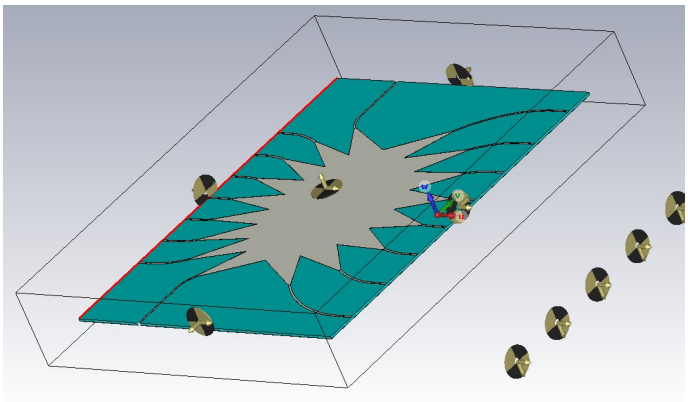


Figure 3.18 – Rotman lens in the S-parameter simulation software imports the previously developed model and performs a simulation of the S-parameters.

4 RESULTS

In this section, the simulations will be presented, and the results related to what was done in Section 3 will be discussed.

4.1 SPDT SIMULATIONS

As previously presented, Keysight's *Advanced Design Systems* program and its resources were used to perform all the simulations for this project. The simulations were performed in the environment *Schematic* – which considers substrate losses and impedance mismatch – and *Layout* – simulation of currents in the mesh by the method of moments. All meshes were simulated with 100 elements per wavelength for the maximum frequency of 15.5 GHz.

4.1.1 Circuit with ideal biasing

The circuit in Section 3.2.6 was first created in the *Schematic* environment and optimized. The circuit configuration with the optimization results was transported to the *Layout* environment, where it was optimized again with electromagnetic simulations. There the circuit improved once more for the lowest insertion loss.

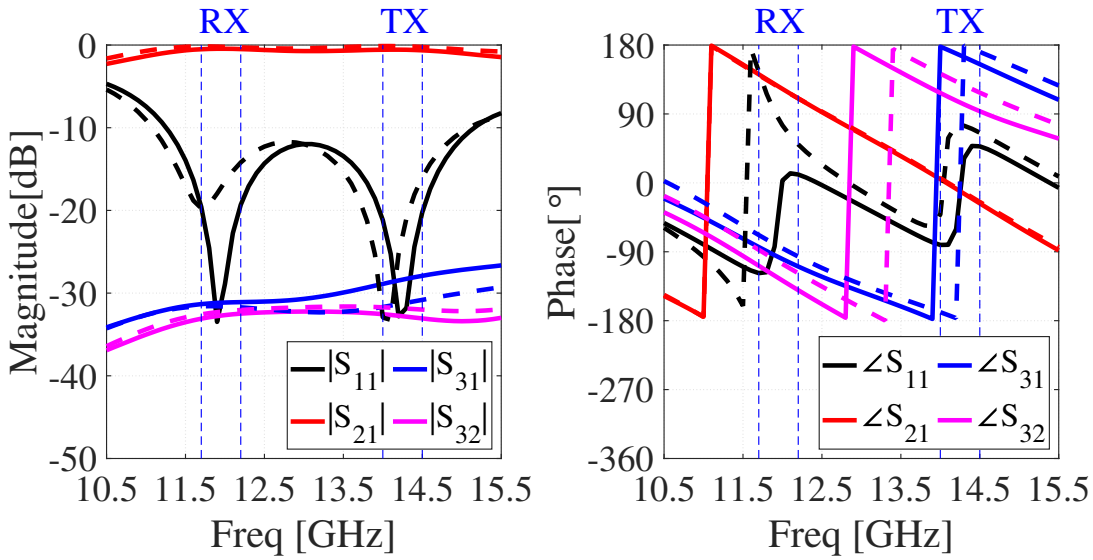


Figure 4.1 – Simulation of the S parameters (magnitude in dB and phase) of the SPDT circuit with ideal biasing with EM simulation in continuous line (—) and schematic simulation in dotted line (- -). Source: Own elaboration.

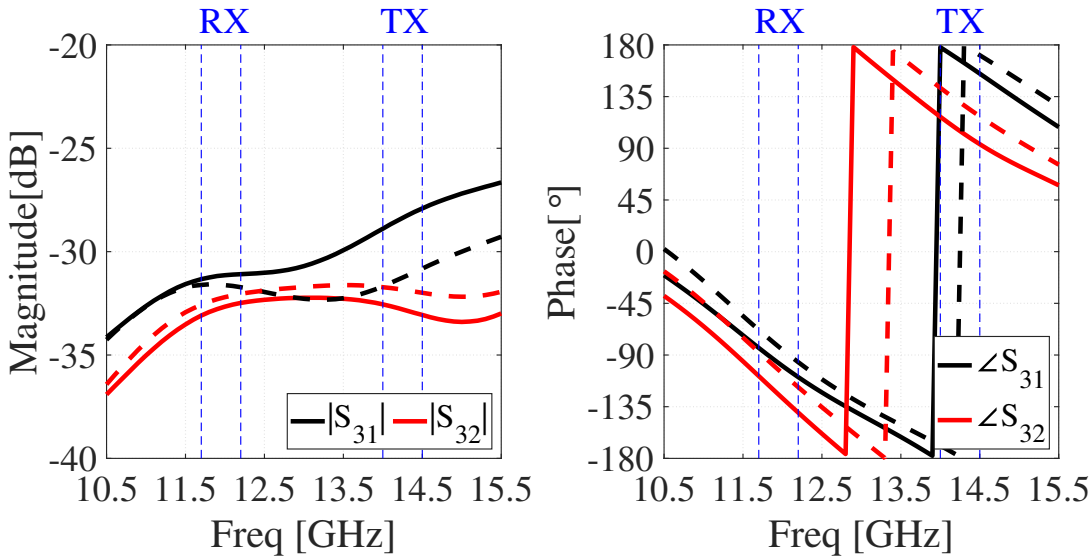


Figure 4.3 – Simulation of parameters S_{31} and S_{32} – isolation between channels – (magnitude in dB and phase) of optimally biased SPDT circuit with EM simulation in continuous line (—) and simulation dotted line schematic (- -). Source: Own elaboration.

The results are in Figure 4.1. In dotted are the schematic results, and in solid line are the S parameters of the electromagnetic simulation. When using the diode, it was necessary to use the LSSP. The Transmit and Receive bands are depicted as vertical blue dotted lines. The most noticeable change was the RL (S_{11}), in which the result of the EM simulation is better than the circuit in the schematic due to the optimizations.

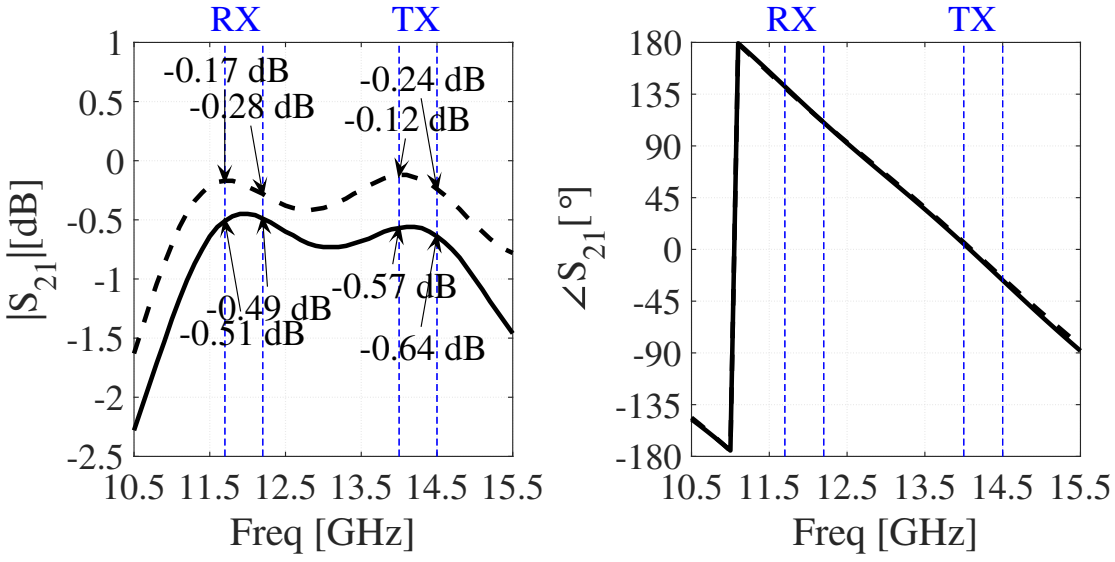


Figure 4.2 – Simulation of parameters S_{21} (magnitude in dB and phase of insertion loss) of the SPDT circuit with ideal biasing with EM simulation in continuous line (—) and schematic simulation in dotted line (- -). Source: Own elaboration.

Power transfer from one port to the other is essential. For the simulations, an RF source

with a power of 35 dBm was used, which is approximately equivalent to 3 W. This was tested in case there is a need to increase the rated power in the transmission, which is up to 33 dBm (2 W).

Figure 4.4 shows power transmission from port 1 to ports 2 and 3 when port 2 is on, and port 3 is off. In it, with few differences between the schematic and the EM simulation, it is possible to notice that almost all the power is destined to the on port (approximately 2.7 W), and very little is transmitted to the off port (approximately 0.005 W).

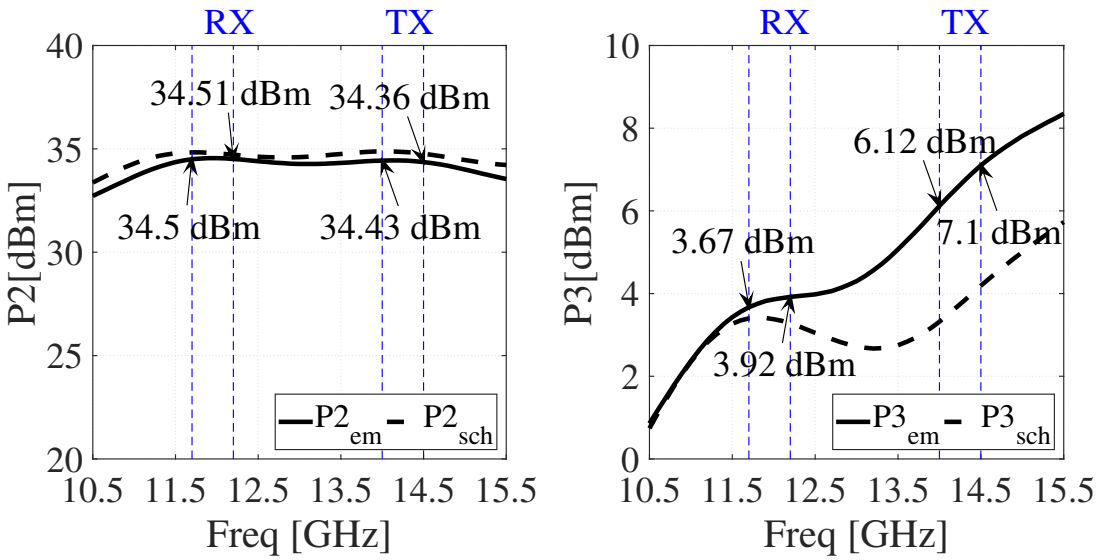


Figure 4.4 – LSSP simulation of optimally biased SPDT circuit with continuous line EM simulation (—) and dotted line schematic simulation (- -) for RF power transmitted to ports 2 and 3 from a 35 dBm. Source: Own elaboration.

4.1.2 Bias Tee

The bias tee described in Section 3.2.6.1, like the previous circuits, had its circuit creation first in the schematic. This electronic system must avoid passing the Rf signal to the DC source and vice versa. The circuit has four ports because one of the diodes in the pair will be connected directly to “T”. Ports 1 and 2 are for passing the RF signal, port 3 for connecting to the diode, and port 4 for the DC source.

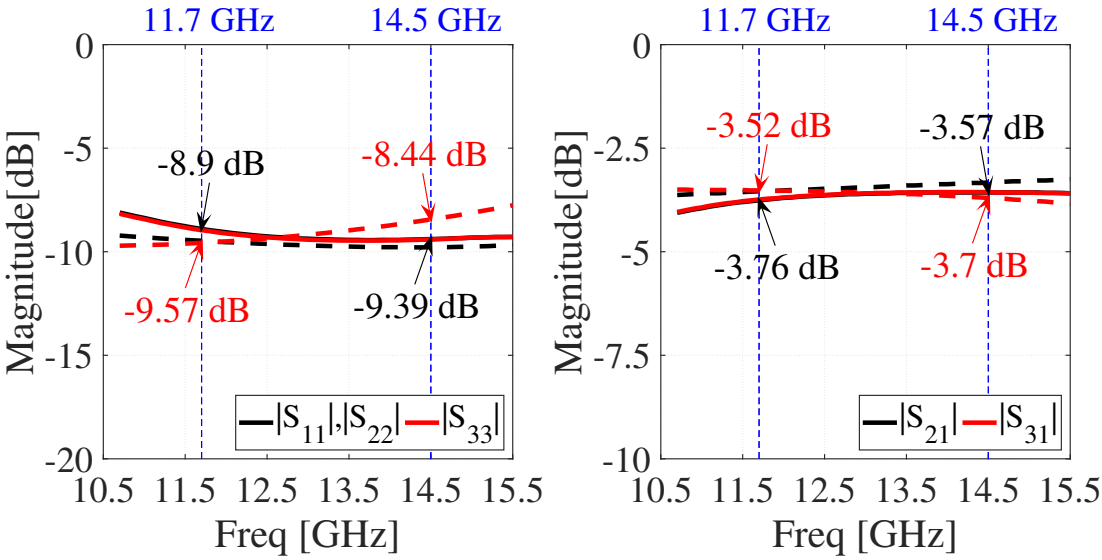


Figure 4.5 – Simulation of S parameters of the bias tee. Left return losses on ports 1, 2, and 3. Right transmission from port 1 to ports 2 and 3. The continuous line for EM simulation (—) and dotted line schematic for simulation (- -). Source: Own elaboration.

Figure 4.5 shows the return loss for ports 1, 2, and 3 together with the transmission from port 1 to ports 2 and 3. Ideally, despite being the same, the parameters S_{21} and S_{31} should also equal 3 dB. This is explained by Figure 4.6.

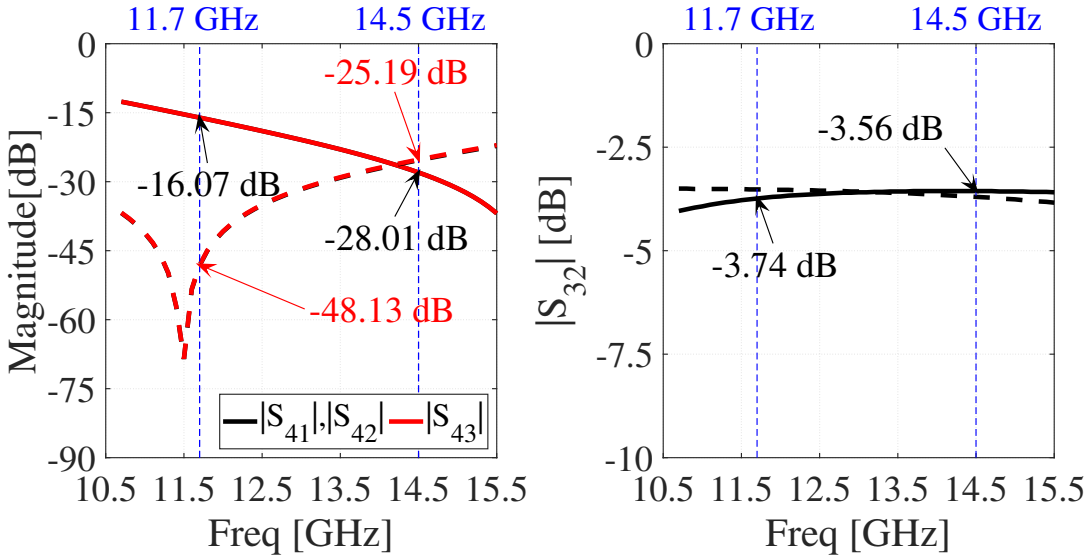


Figure 4.6 – Simulation of S parameters of the bias tee. Left transmission from port 4 to ports 1, 2, and 3. Right transmission from port 3 to port 2. The continuous line for EM simulation (—) and dotted line for schematic simulation (- -). Source: Own elaboration.

Figure 4.6 shows the difference between the EM simulation and the schematic level. Even after optimization rounds, the parameters S_{41}, S_{42} and S_{43} remained high, showing that part of the signal is shunted to ports 2 and 3, causing S_{21} and S_{31} to stay greater than 3 dB.

4.1.3 Diode Bias

The diode bias circuit presented in Section 3.2.6.1 has only one port, which is the connection with the PIN diode. So the only parameter available is S_{11}. For its operation, it is necessary that the RL is as large as possible (closer to 0 dB).

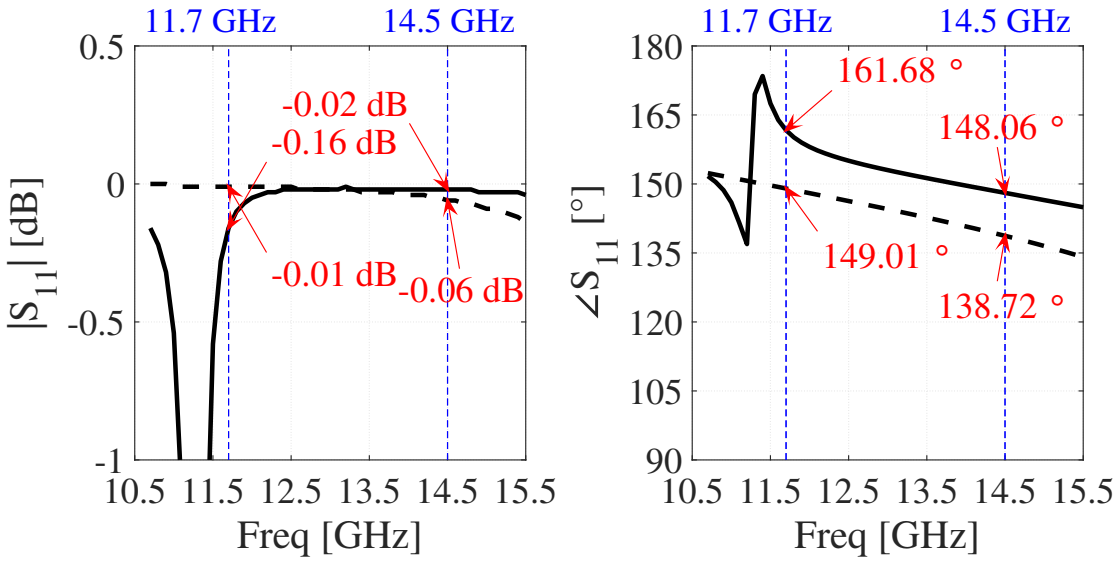


Figure 4.7 – Simulation of the parameter S_{11} of the diode bias with a resistor of $50\,\Omega$. The solid line for EM simulation (—) and dotted line for schematic simulation (- -). Source: Own elaboration.

Although the schematic simulation curves are different from the EM simulation curves, the results for the diode bias circuit are satisfactory, as they present a high return of RF power to port 1.

4.1.4 Full circuit

Now with the individual circuits simulated and optimized separately, all circuits are put together, simulated, and optimized again. The results are shown in Figure 4.8.

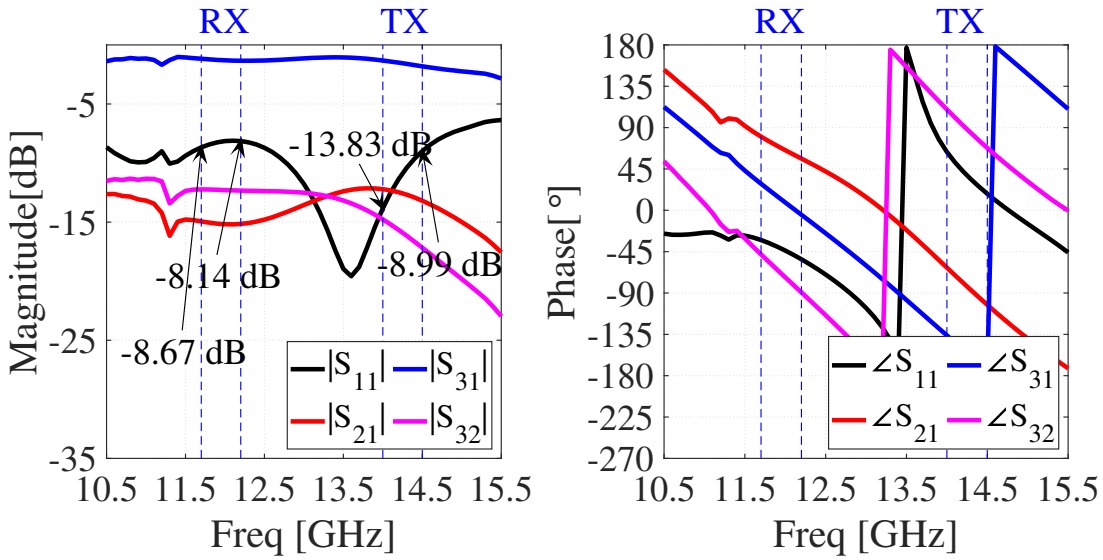


Figure 4.8 – LSSP (magnitude in dB and phase) simulation of the SPDT circuit with projected bias. Port 1 as RF signal source, port 2 off, and port 3 on for RF signal passing. Source: Own elaboration.

As expected, it was observed in Figure 4.8 that there is a worsening of performance in relation to the simulation of Figure 4.1. This is due to the designed bias circuits, which are not ideal lossless models. As with the other simulations that include diodes, the LSSP was used. All simulations present the scenario of port 1 as RF source, port 2 off, and port 3 on for the passage of the RF signal.

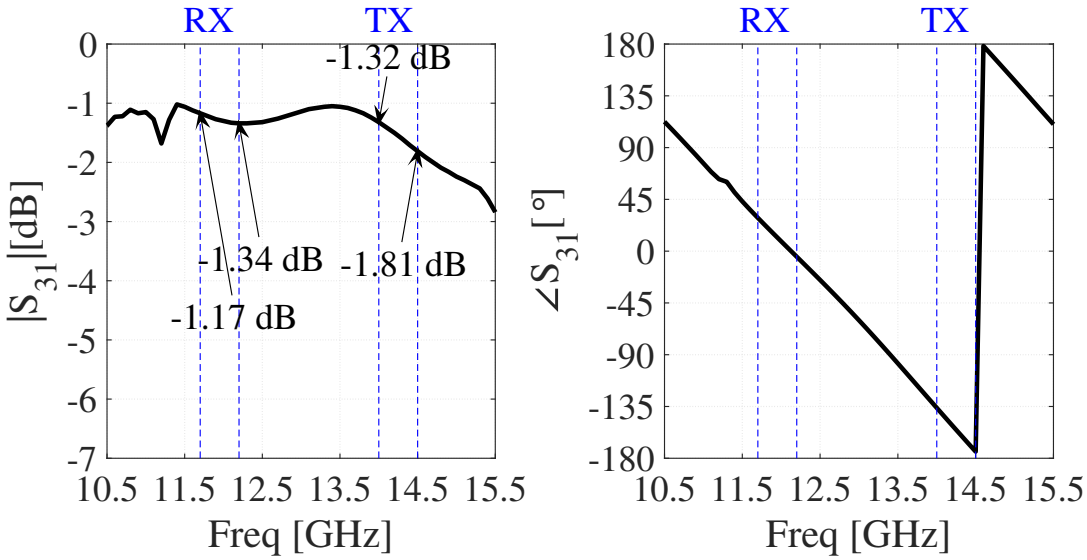


Figure 4.9 – LSSP simulation (magnitude in dB and phase) for parameter S_{31} of SPDT circuit with projected bias. Port 1 is the source of the RF signal and port 3 is connected for the passage of the RF signal. Source: Own elaboration.

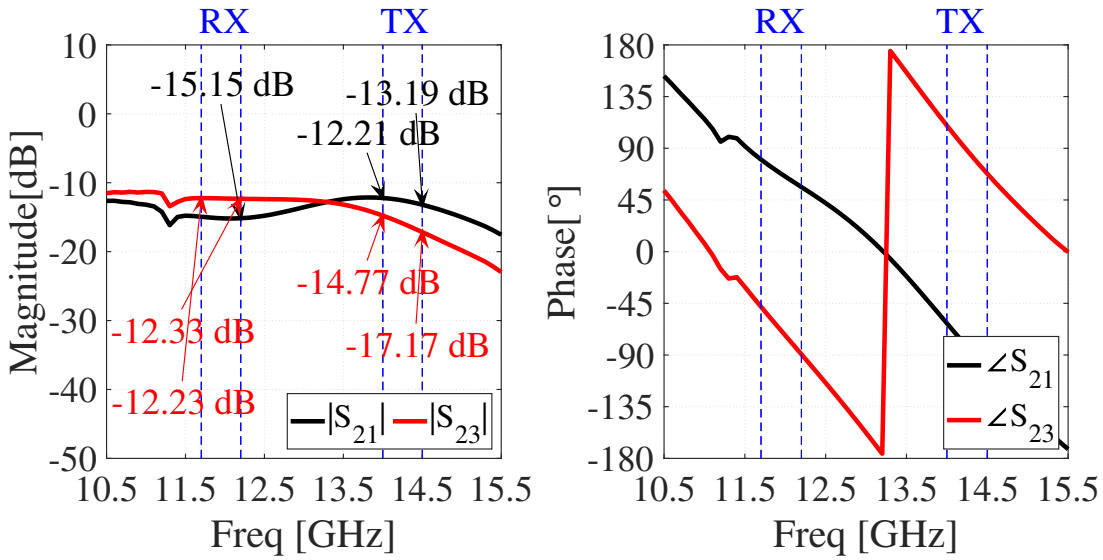


Figure 4.10 – LSSP simulation (magnitude in dB and phase) for the parameter S_{21} and S_{23} of the SPDT circuit with projected bias. Port 1 is the source of the RF signal and port 3 is connected for the passage of the RF signal. Source: Own elaboration.

The results for the RF power transmission (Figure 4.11) are also worse than those seen in Figure 4.4.

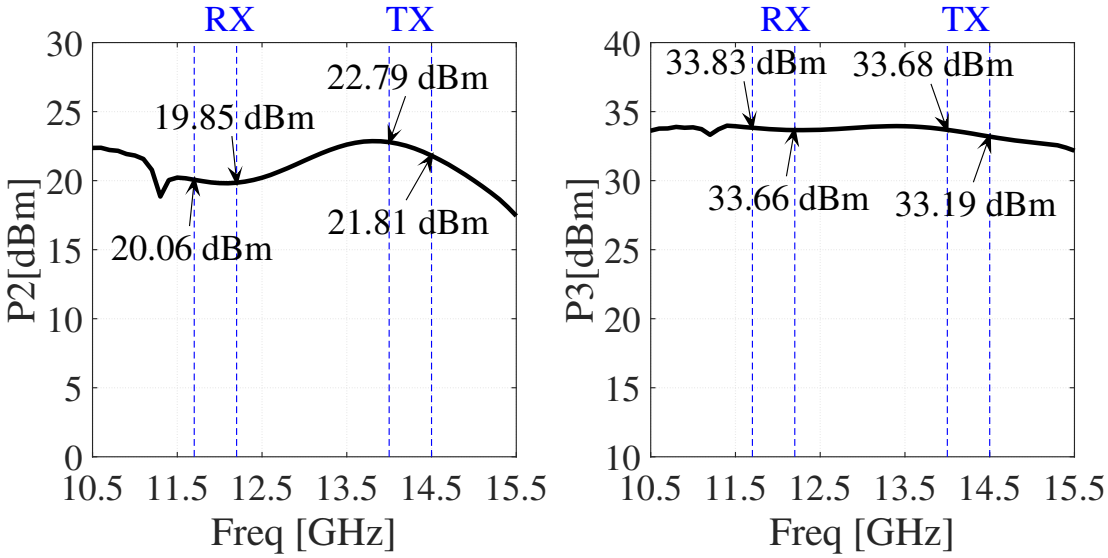


Figure 4.11 – LSSP simulation of SPDT circuit with bias designed for RF power transmitted to ports 2 and 3 from a source of 35 dBm. Source: Own elaboration.

4.1.5 Circuit printed on board

After finalizing the RF switch design, the circuit was placed in the design of the transceiver boards and passive components. Access lines and *pads* were also placed with it for the SMA connectors.

The final set was exported from the printed circuit board design program and simulated again with the ADS program.

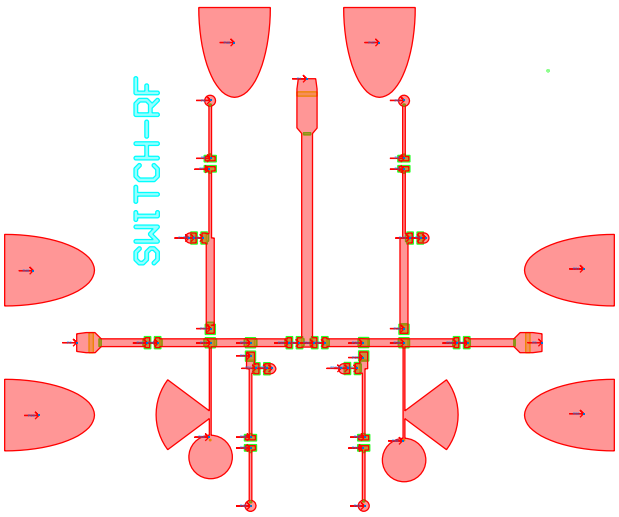


Figure 4.12 – RF switch circuit imported from the software PCB creation for the ADS *Layout* environment. Source: Own elaboration.

Although there is a similarity between the curves in Figures 4.12 and 4.8, there was a compromise in the switch performance due to the pads of the connectors and the new lines access on microstrip (Figures 4.14,4.15 and 4.16). Even so, the switch was sent to the manufacturer.

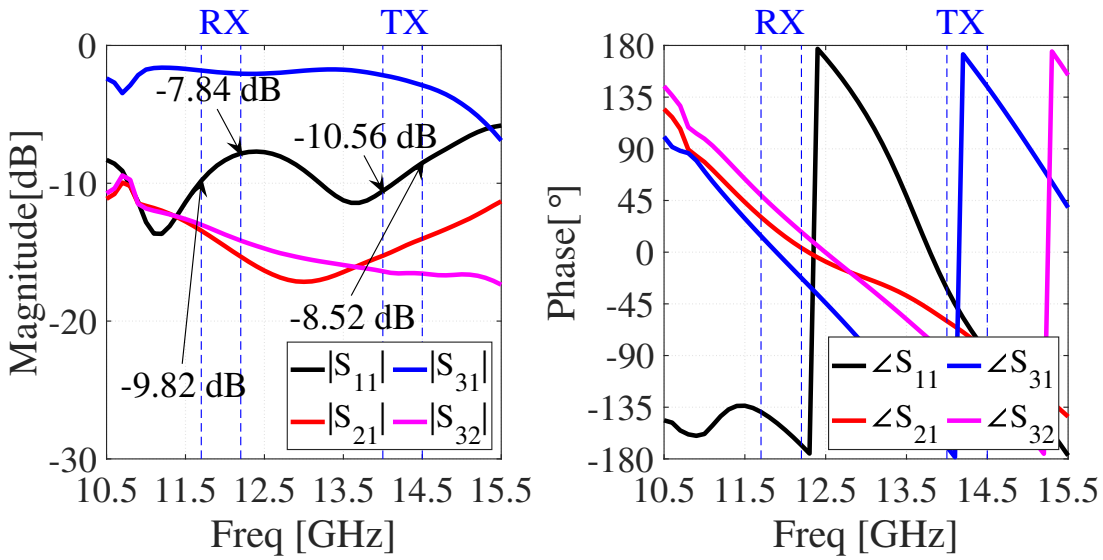


Figure 4.13 – LSSP (magnitude in dB and phase) simulation of the imported circuit. Port 1 as RF signal source, port 2 off, and port 3 on for RF signal passing. Source: Own elaboration.

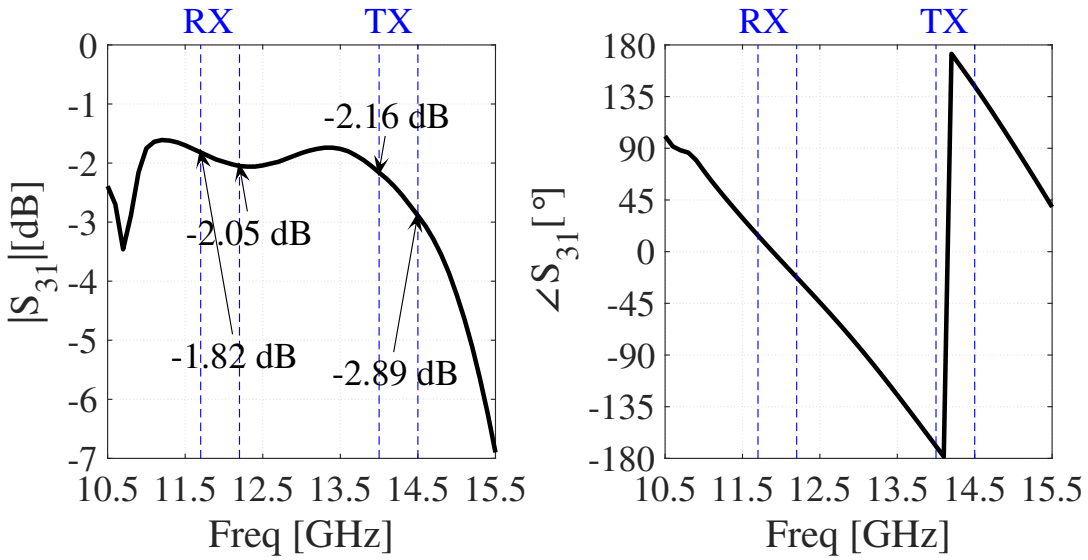


Figure 4.14 – LSSP simulation (magnitude in dB and phase) for the parameter S_{31} of the imported circuit. Port 1 is the source of the RF signal and port 3 is connected for the passage of the RF signal. Source: Own elaboration.

These simulations (Figures 4.14,4.15 and 4.16) show good results for the designed switch already placed on the PCB.

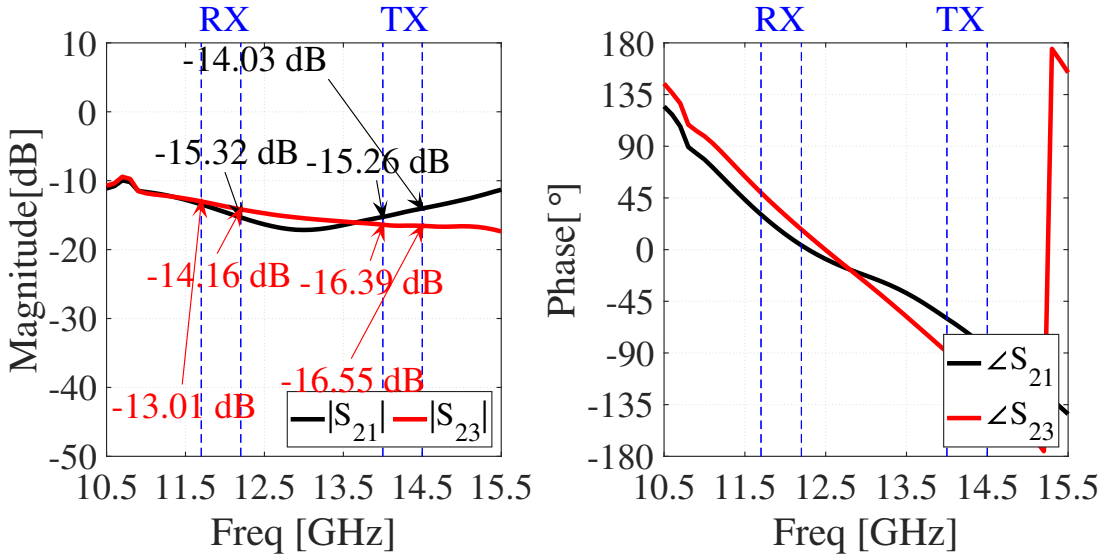


Figure 4.15 – LSSP simulation (magnitude in dB and phase) for the imported parameter S_{21} and S_{23}. Port 1 is the source of the RF signal and port 3 is connected for the passage of the RF signal. Source: Own elaboration.

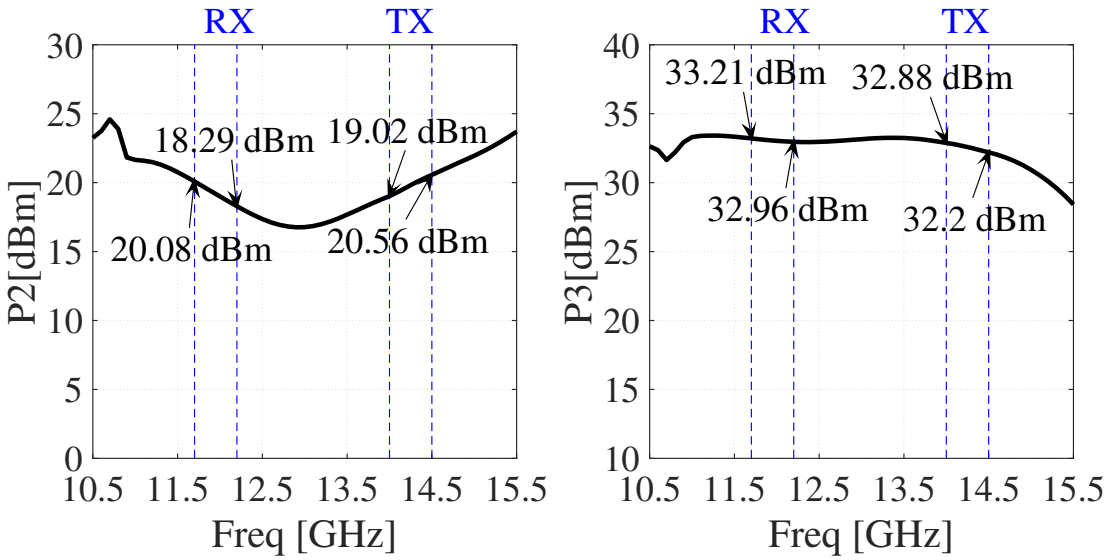


Figure 4.16 – LSSP simulation for power transferred from port 1, at 35 dBm, to ports 2 and 3. Port 1 is the RF signal source, and port 3 is connected for RF signal passage. Source: Own elaboration.

This last simulation was done together with a DC simulation to verify the currents that polarize the diodes (Table 4.1). This was mainly set to evaluate if the currents are close to exceeding the limit imposed by the datasheet.

Table 4.1 – Values in magnitude of the currents over the diodes during DC simulation. Source: Own elaboration.

Diodes	Diode #1	Diode #2	Diode #3	Diode #4
Current	$643,3$ uA	$92,5$ uA	$1,2$ mA	$698,2$ uA

4.2 SPDT ANALYSIS AND PCB

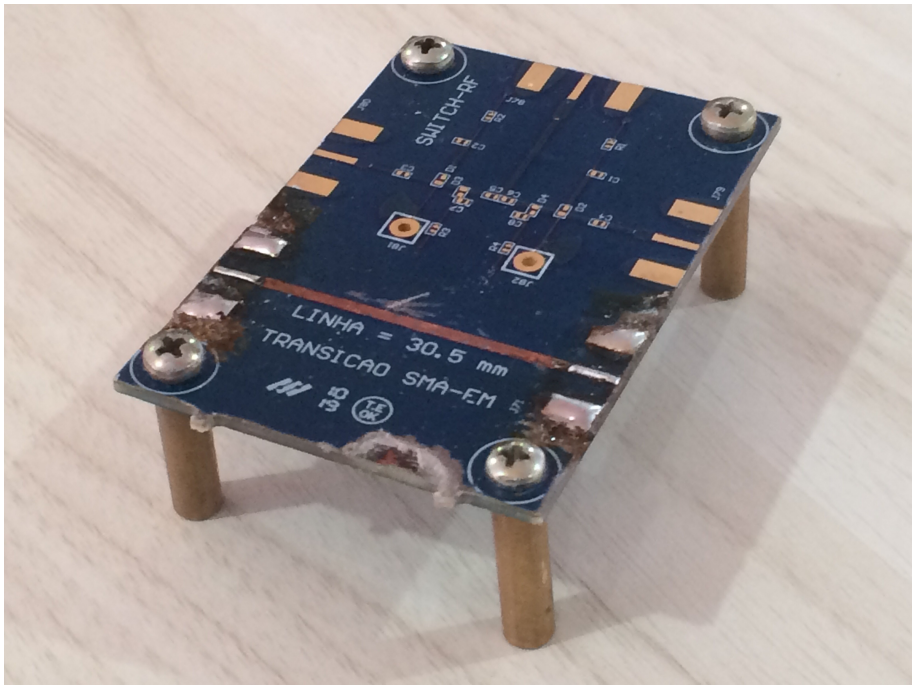


Figure 4.17 – Photograph of the board with the switching circuit in perspective. Source: Own elaboration.

The design of this switching circuit, even if only one element of the matrix, is essential for the rest of the system. It will be possible to identify faults to be corrected for the matrix and verify if the applied theory is compatible with the simulated results and the results extracted from the printed circuit.

The switch circuit was manufactured by Micropress (Figure 4.21). Unfortunately, after receiving the plates (Annex D) several defects were observed in several microstrip tracks. In addition, several of the trails were deleted (Figures 4.21, 4.22 and 4.23) and others that should have been isolated were connected. This may have happened due to a lack of control of copper corrosion during the process.

Likewise, in tests of a single microstrip track from SMA to SMA, the lack of grounding that should be connected via through hole was noticed. However, these defects were observed in many circuits, and neither the RF switch nor other passive circuits (filters, transitions) were tested.

Some of the measures that can be taken concerning these defects are to work away from the limits described by manufacturers. Another measure would be for the circuit to undergo an evaluation process before its manufacture together with the engineers responsible for the manufacturing process and more outstanding care during it.

The last option would be to change the manufacturer. Unfortunately, in Brazil, the

only company with technical capacity at the moment was Micropress, which works with AD250C™(Figure 4.25), requiring the use of an international manufacturer. This raises the cost of labor and other charges due to imports and taxes. Therefore, this is the last option to consider.

As for the errors made by the manufacturer, a report of the factors that made it possible to have inferior quality boards was requested, together with another report of the changes to be made to facilitate the manufacturing process. New versions of the boards and the switching circuit are already being designed.

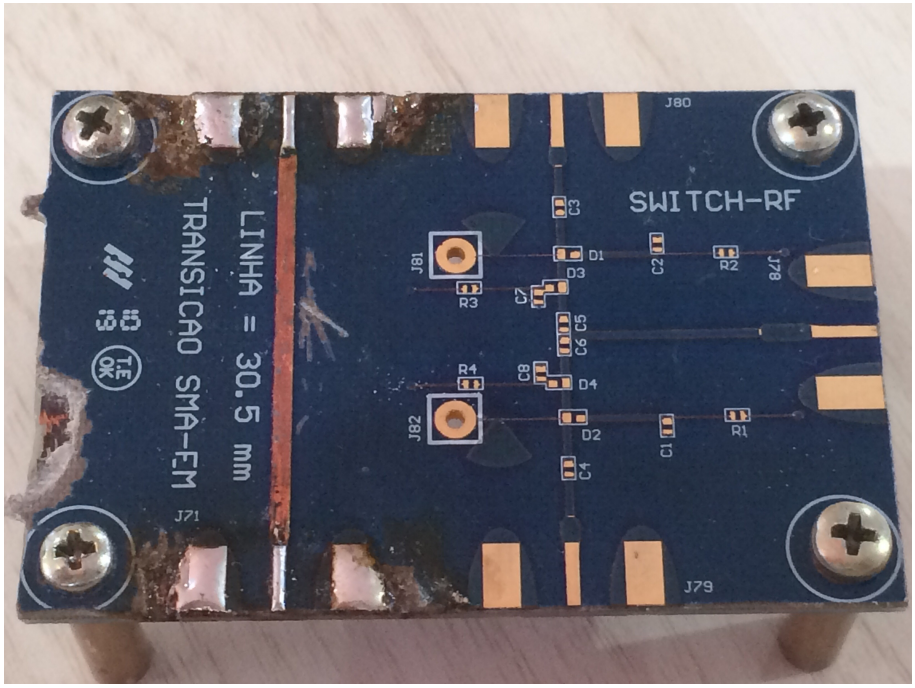


Figure 4.18 – Photograph of the board with the switch circuit on the right and the transition line on the left in the top view. Source: Own elaboration.

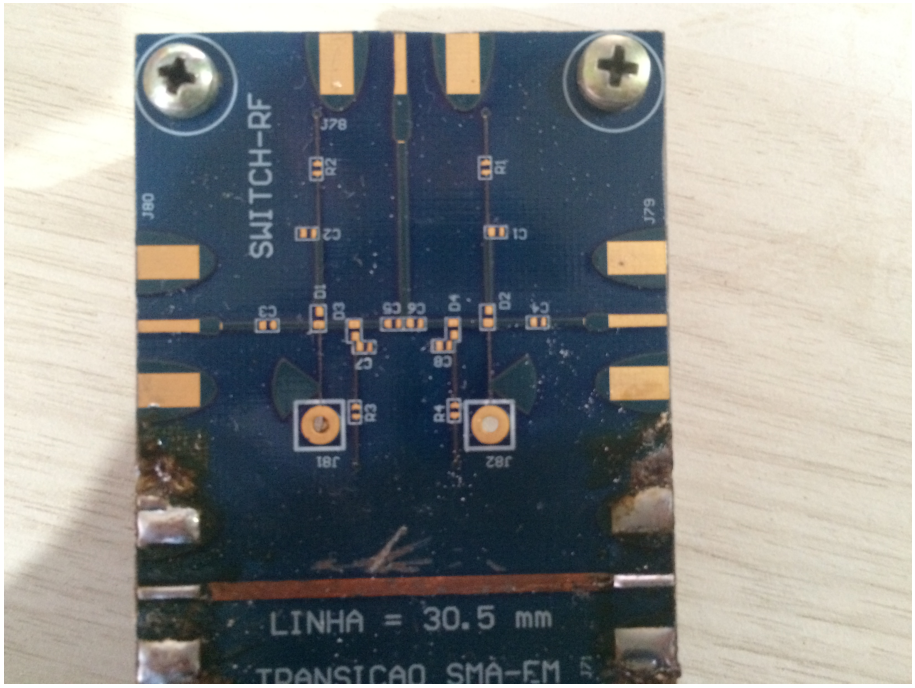


Figure 4.19 – Photograph of the switching circuit with port 1 vertically and ports 2 and 3 horizontally, on the left and right, respectively. Source: Own elaboration.

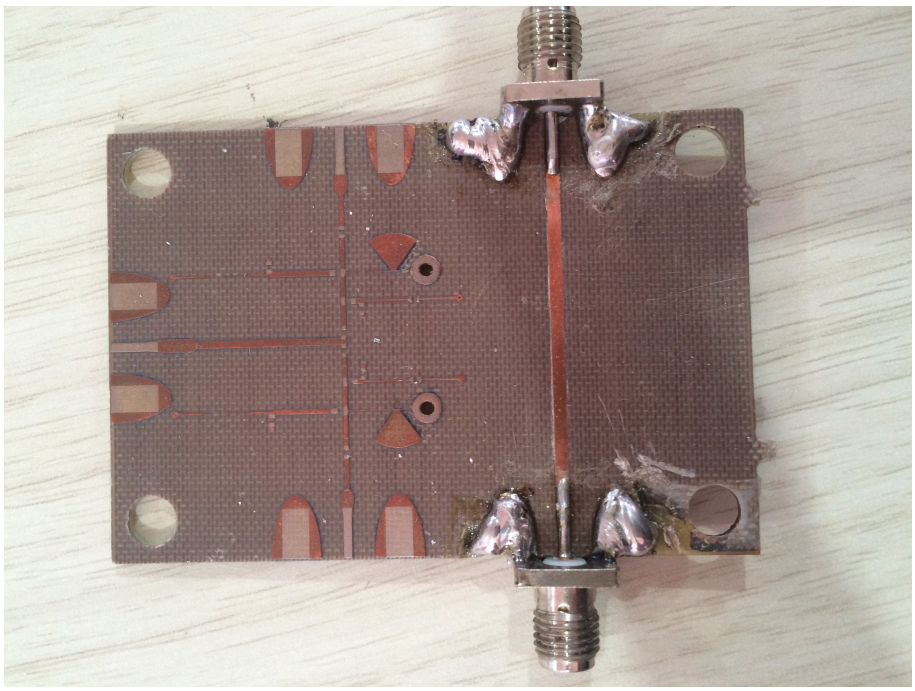


Figure 4.20 – Top view photograph of the switch circuit without solder mask. Source: Own elaboration.

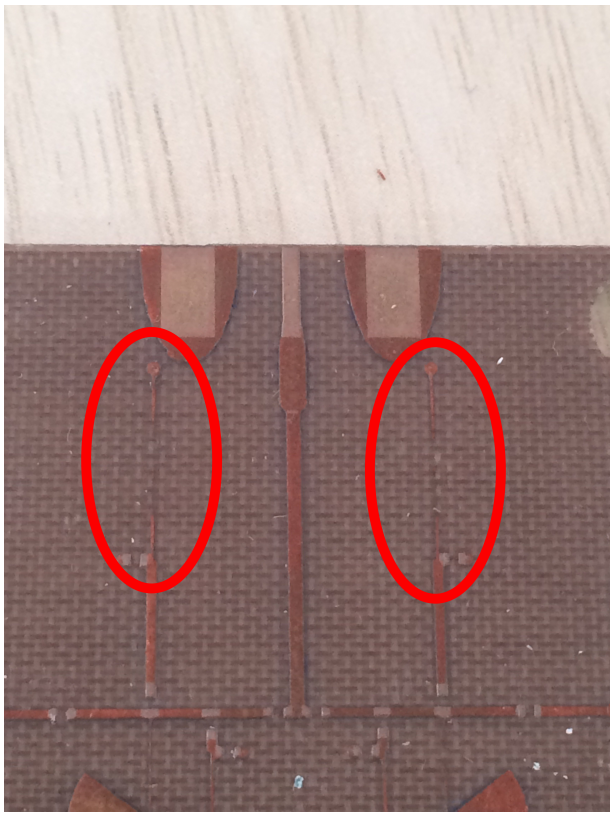


Figure 4.21 – Top view photograph of the switch circuit without solder mask with removed microstrip tracks circled in red due to the manufactured process. Source: Own elaboration.

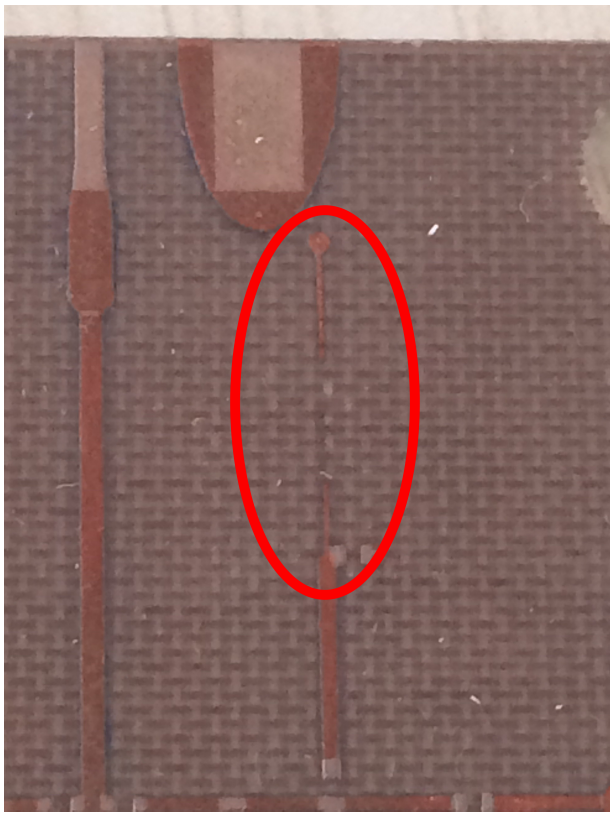


Figure 4.22 – Photograph of the switching circuit with red detail fault in the microstrip track that polarizes the right channel. Source: Own elaboration.

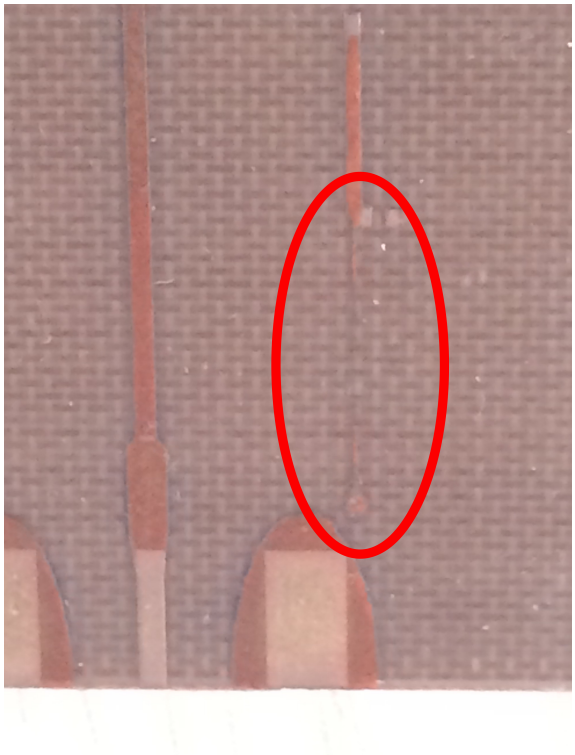


Figure 4.23 – Photograph of the switching circuit with red detail fault in the microstrip track that polarizes the left channel. Source: Own elaboration.

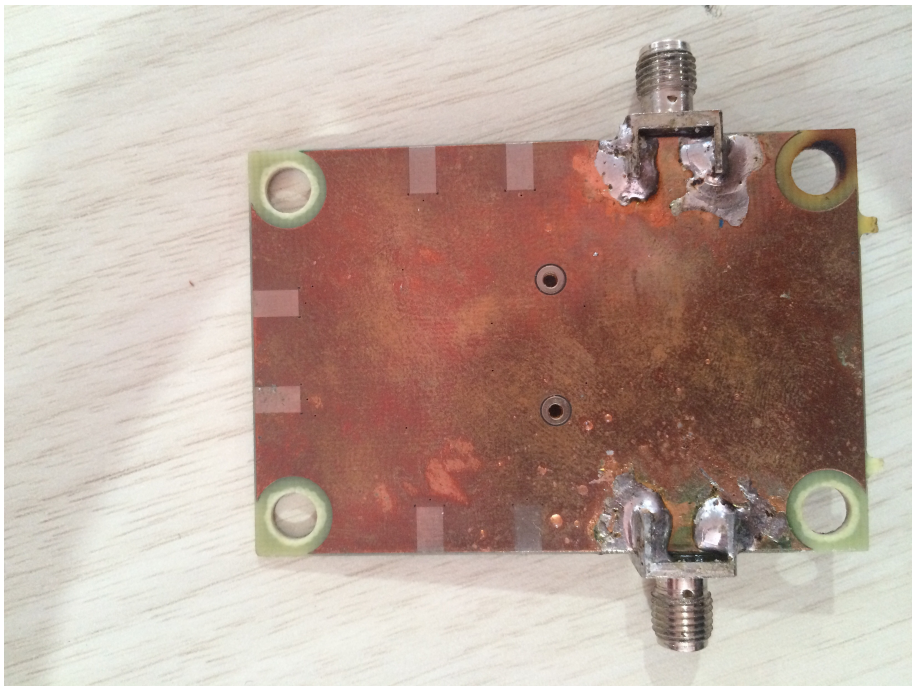


Figure 4.24 – Photograph of the switching circuit in bottom view without solder mask. Source: Own elaboration.

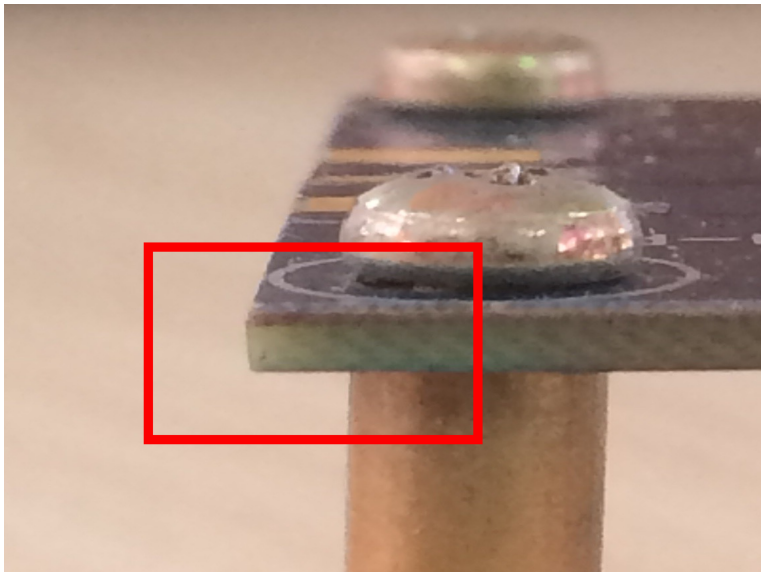


Figure 4.25 – Photograph of the switching circuit in side view showing the two layers of substrate, the lighter and lower one being FR4 and the darker one and the upper one being AD250C. Source: Own elaboration.

There was a second round of manufacturing free of charge due to manufacturing errors. Boards were made in it, with active and passive circuits (such as filters, transitions) and SPDT again. Despite the need for fast shipping, version 1 of SP4T was included (Annex C.1), taking advantage of the available space.

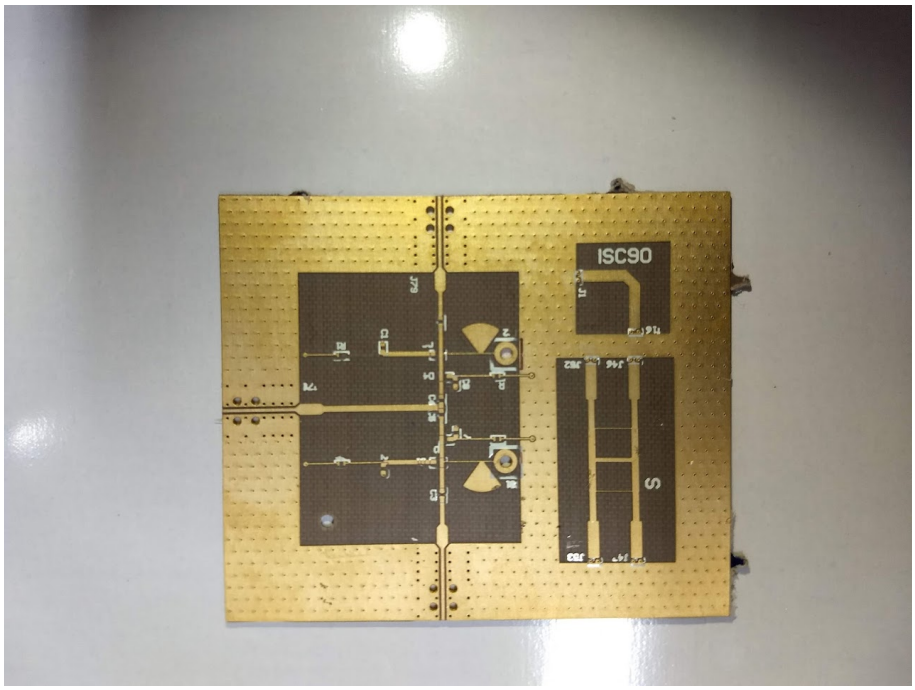


Figure 4.26 – Photograph of the SPDT switching circuit from the second round of fabrication in top view showing the ground plane and ways to maintain the equipotential ground plane. Source: Own elaboration.

Vias have been added to keep the ground plane fluctuating across the board. Unfortunately, even with care during manufacturing, a control track was eroded too much (Figure 4.26), leaving it open. This again made the SPDT test impossible.

4.3 SP4T SIMULATIONS

As with SPDT, in SP4T, all simulations were performed using Keysight's *Advanced Design Systems* program and its resources. The simulations were performed in the environment *Schematic* – which considers substrate losses and impedance mismatch – and *Layout* – simulation of currents in the mesh by the method of moments. All meshes were simulated with 100 elements per wavelength for the maximum frequency of 17 GHz.

Only electromagnetic simulations by the method of moments between 9 GHz and 17 GHz will be presented in this section since it is proven that the schematic simulation works. However, it is not as faithful as the EM simulation performed in the *Layout* environment.

4.3.1 Bias tee with stub double radial

Because it has a wide band, the insertion loss of the bias tee is relatively high (between -0.4 dB and -0.7 dB). Despite this, the RL remains below -13 dB, and isolation for the DC

signal port (Port 3) is below -30 dB. Less than one-thousandth of the RF power reaches the DC control source.

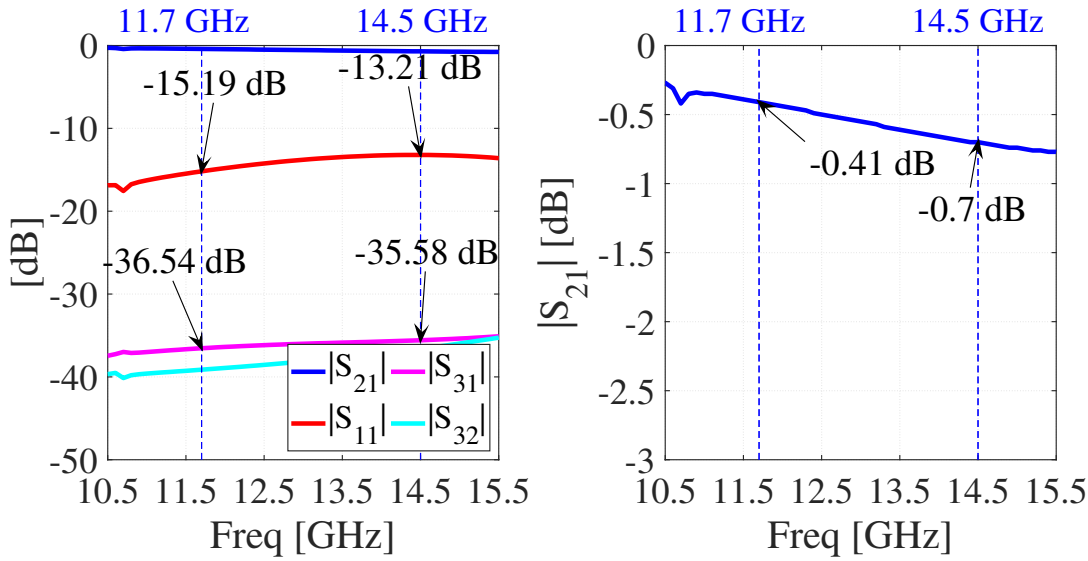


Figure 4.27 – Simulation of the S parameters of the biasing circuit with two radial *stubs* in EM simulation. On the left S_{11}, S_{21}, S_{31} and S_{32}, and on the right the IL represented by the parameter S_{21} . Source: Own elaboration.

4.3.2 Full circuit SP4T

With the new bias tee model, it was possible to simulate and optimize the complete circuit of SP4T v2.0. After optimization, all ports had similar S parameters.

In Figure 4.29 it is observed that the RL is below -13 dB in the entire band. A loss is considered good if the manufacturing has similar values.

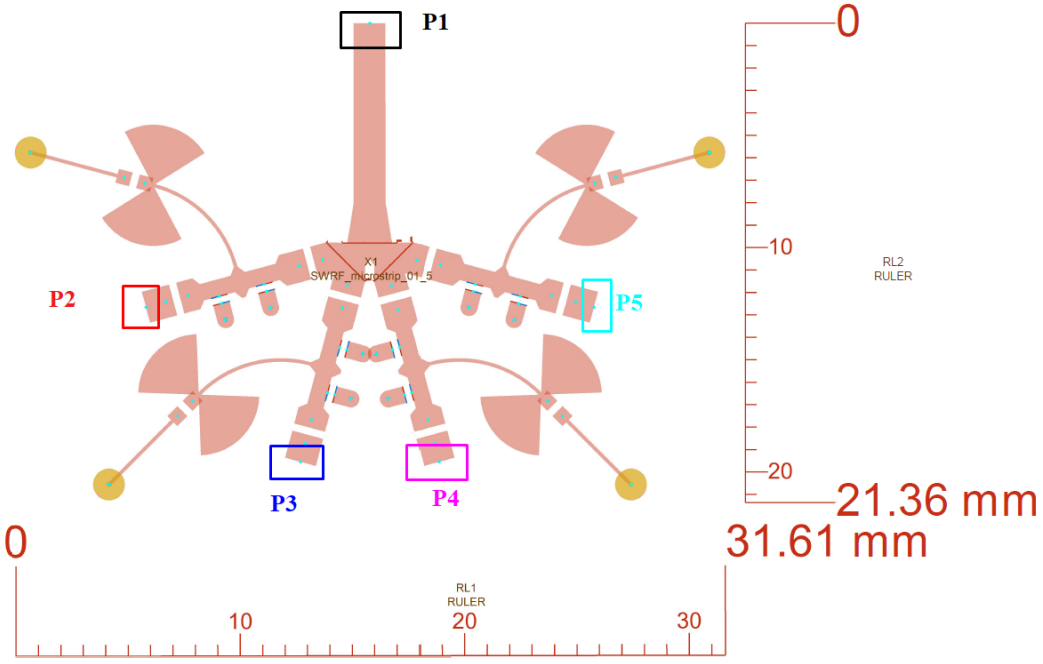


Figure 4.28 – Switching circuit SP4T version 2.0 in complete microstrip in the *Layout* environment shows the switch's measures and the ports (P1 as central and P2 to P5 for the other channels). Source: Own elaboration.

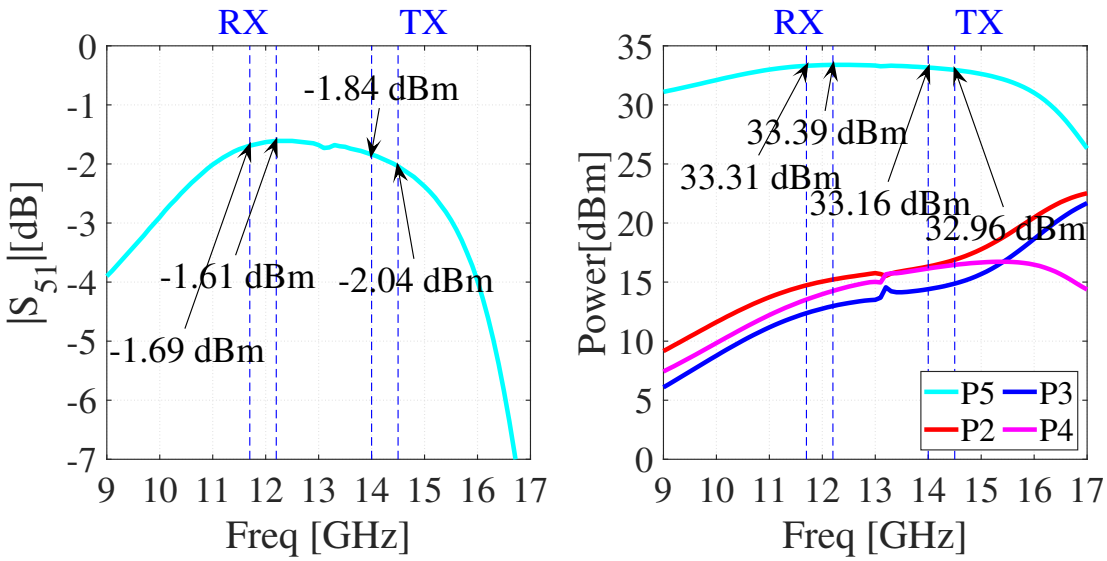


Figure 4.30 – SP4T v2.0 LSSP simulation for port 1 as 35 dBm RF signal source and port 5 connected for RF signal pass. On the left is the IL, and on the right are the powers that reach all ports. Source: Own elaboration.

The insertion loss seen in Figure 4.30 is approximately 2 dB, considered adequate for the bandwidth and number of channels. This result is significant for Microwave switch array (MSA) to have the lowest possible IL. When injected with the signal of 35 dBm with port 5 ON, a signal with 33 dBm is obtained, and in other ports, only 15 dBm.

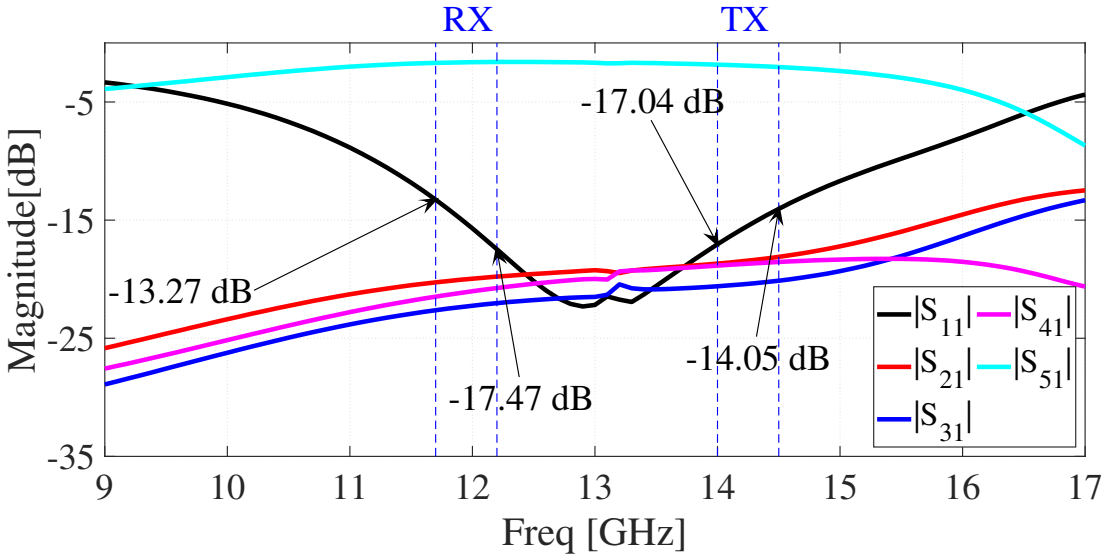


Figure 4.29 – SP4T v2.0 LSSP simulation for powers transferred from port 1 to ports 2, 3, 4, and 5. Port 1 is the source of the RF signal and port 5 is connected to pass the RF signal. Source: Own elaboration.

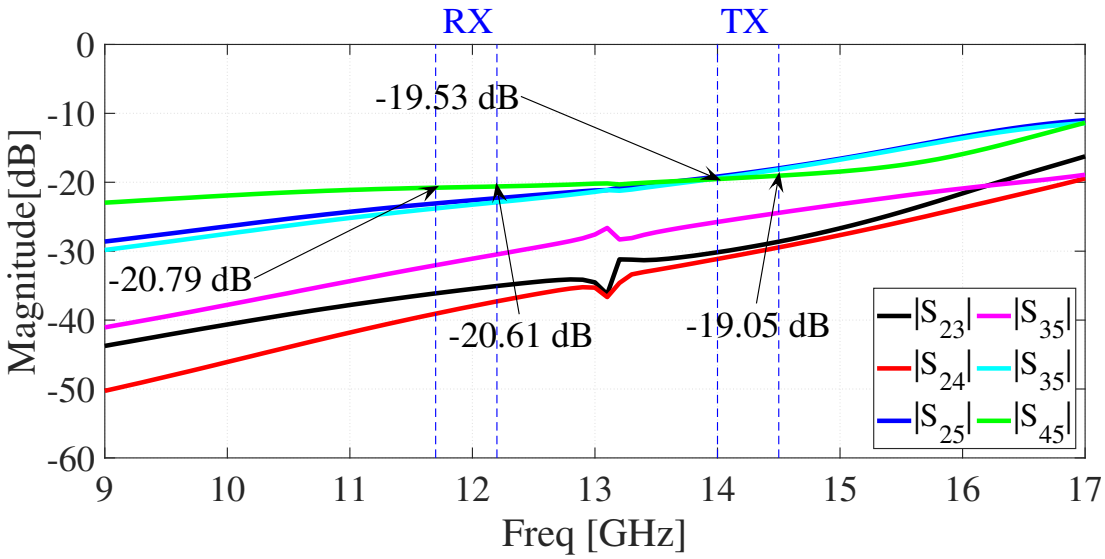


Figure 4.31 – SP4T v2.0 LSSP simulation showing isolation between ports with port 1 as the RF signal source and port 5 turned on for RF signal passing. Source: Own elaboration.

Interchannel isolations are, as expected, close to or less than -19 dB. This result is also crucial for the pointing system to have a clean beam diagram.

Analyzing the graphs above and comparing them with the SPDT results showed a significant improvement in all aspects (IL, ISO, and RL) and a reduction in losses. In addition, there was some improvement of 1 dB in the IL for the transmitting channel, as the number of channels passing through the switch was doubled.

SP4T v2.0 was placed on the passive elements board along with filters, couplers, res-

onators, bypasses, and transitions. This plate was ready for manufacturing.

4.3.3 Statistical Analysis of Performance - Yield

The purpose of Yield is to perform a parametric analysis that tries to predict the different variations of the manufacturing process. This analysis was done on the best 1 to 4 switch (SP4T v2.0) to try to predict behavior after manufacturing defects delimited by the standard.

The analysis of Yield provided by ADS Keysight was performed. The form of random distribution chosen was the Uniform Distribution due to the lack of knowledge of the manufacturer's process. In addition, the limits of $\pm 10\%$ lengths and widths below $250\,\mu$m were respected and limited to a maximum error of $\pm 25\,\mu$m for distances greater than $250\,\mu$m. These data were provided by the manufacturer and are included in the standard.

In this analysis, a set up was done with 250 iterations with variation in only lengths at the end of tracks and widths, except for angles. With Yield (dashed line Y in Figure 4.34), it is possible to check the iterations that meet a requirement. The chosen one was from S_{21} greater than $-2.5\,$dB. The simulation was done to determine if the circuit is robust or not to manufacturing defects.

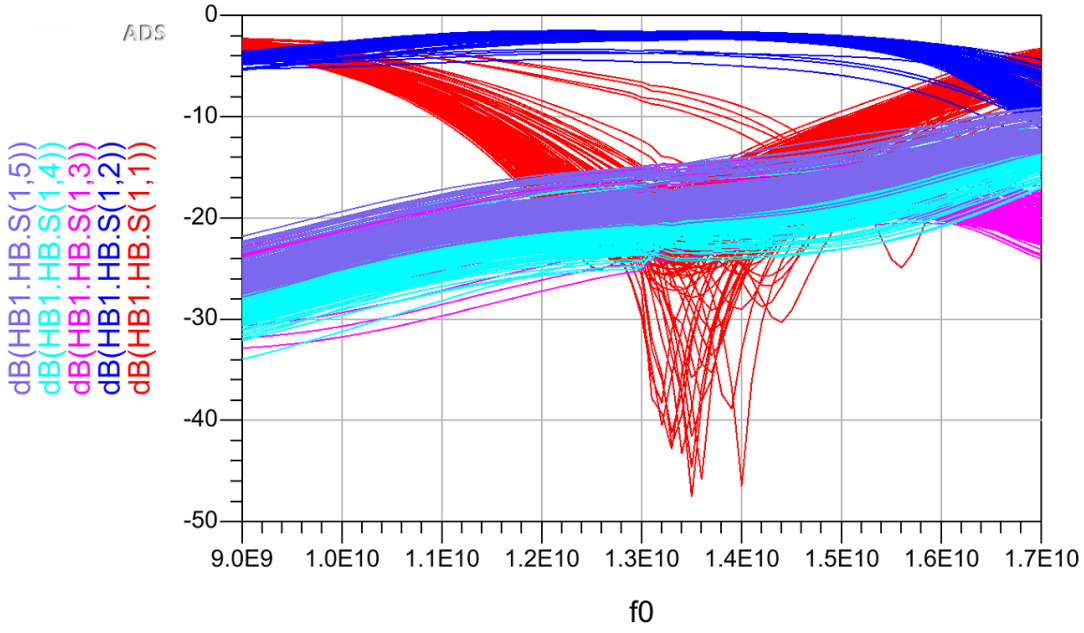


Figure 4.32 – *Yield* analysis for the SP4T v2.0 circuit showing the S parameters for port 1 and 250 iterations. Source: Own elaboration.

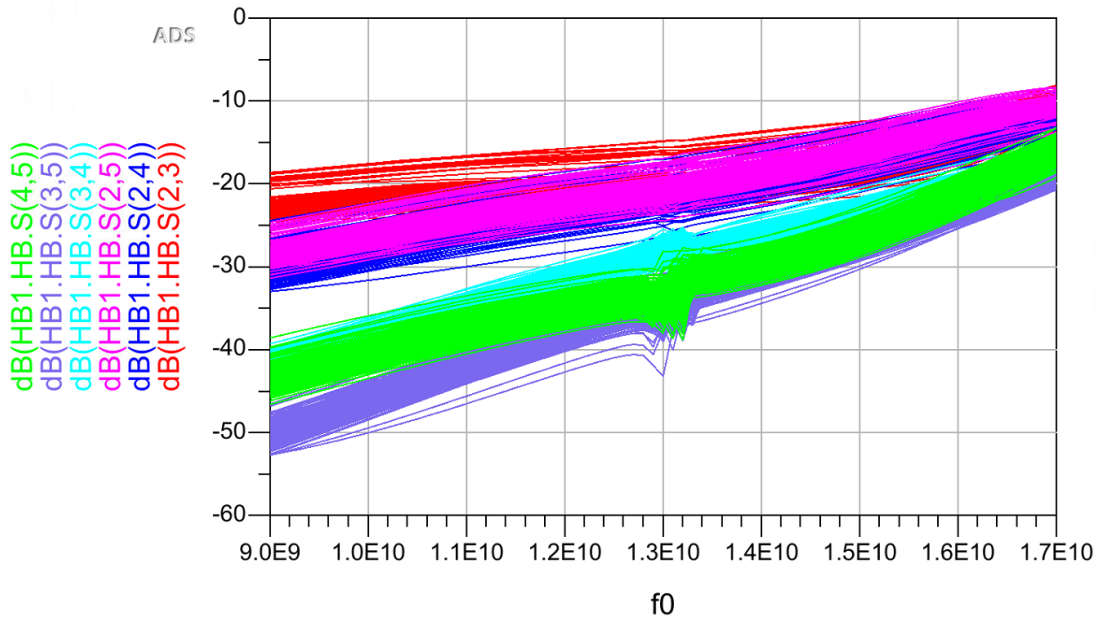
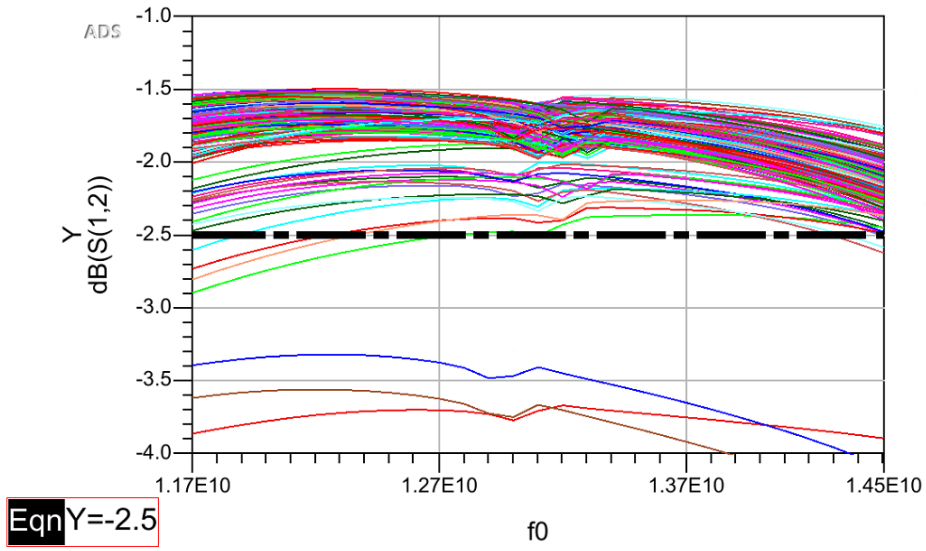


Figure 4.33 – *Yield* analysis for the SP4T v2.0 circuit showing the S parameters for the isolation between the ports and 250 iterations. Source: Own elaboration.

It is possible to notice that only eleven of the 250 iterations of the analysis performed in Figure 4.34 were below the limit of -2.5 dB. This limitation was imposed expecting an acceptable manufacturing deviation of up to 0.5 dB. The *Yield* calculated during this simulation is 95.6%. This represents the proportion of the number of curves that meet the imposed limit.



PPT_Converts	PPT_Yield	PreTuneFail	PreTunePass	PreTuneYield
0.000	95.600	11.000	239.000	95.600

Figure 4.34 – *Yield* analysis for the SP4T v2.0 circuit showing the S_{12} parameter for 250 iterations. Also shown is the line determined for the reliability check at -2.5 dB. Only 11 curves were below the specified value. Source: Own elaboration.

This analysis can verify the reliability of the circuit's yield made for the circuit. According to Keysight Technologies[41] tables, for a yield of 95.6%, there is 68.3% confidence that the result has an error of $\pm 2\%$, that is, be between 93.6% and 97.6%. With a confidence level of 95.4%, the estimated error is $\pm 4\%$, ranging between 91.6% and 99.6%. Increasing the confidence to 99.7%, the error estimate is $\pm 5\%$, with a variation between 90.6% and 100%.

These results show a good level of security for circuit fabrication. With them, it is possible to conclude with 99.7% confidence that there is more than a 90% chance that the circuit has an IL better than -2.5 dB.

4.4 SIMULATIONS MATRIX SP16T

With the significant increase in size, the circuit began to demand much processing, so it was reduced to just two switches cascaded in series, with only eight ports. This does not change the results of the S parameters of the ports and reduces the calculation time of the electromagnetic simulations. The results were quite similar for either port. The results shown are for port 3 ON and the others OFF.

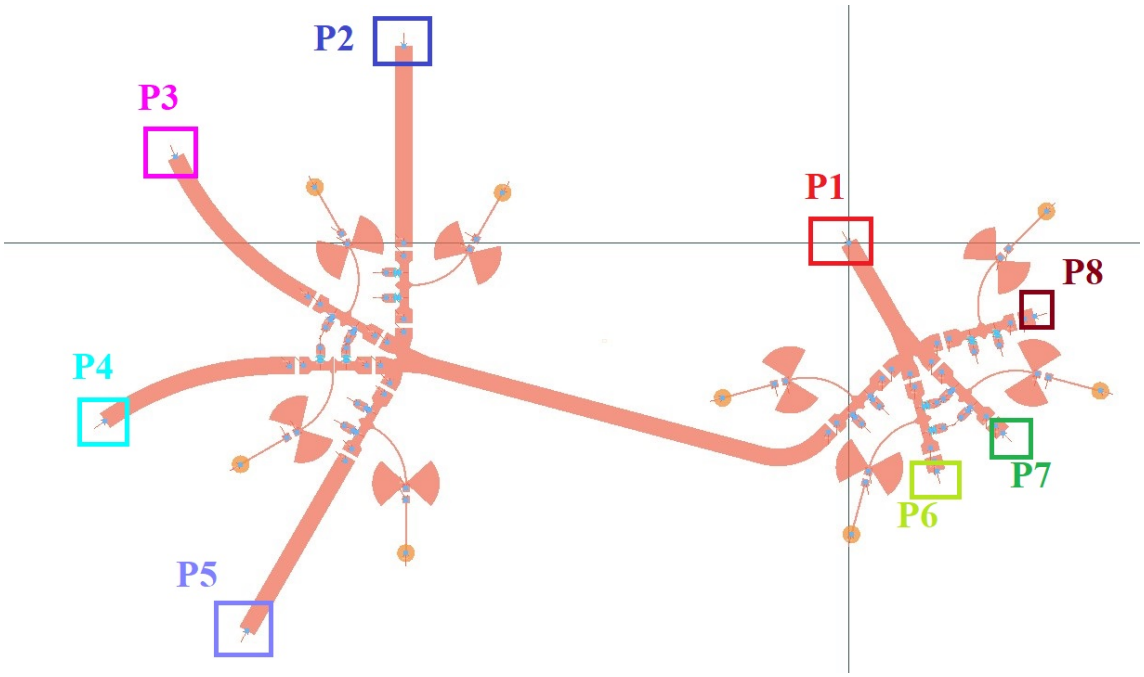


Figure 4.35 – LSSP Layout simulation of the MSA SP16T showing the two SP4Ts v2.0 cascaded due to the need for faster processing. Ports 1 to 8 are also shown. Source: Own elaboration.

Unfortunately, optimizing this circuit was impossible due to the simulation time and the urgency in sending it to manufacturing. Therefore, the worsening in the results (IL, RL, and ISO) shown in Figure 4.36 was already expected.

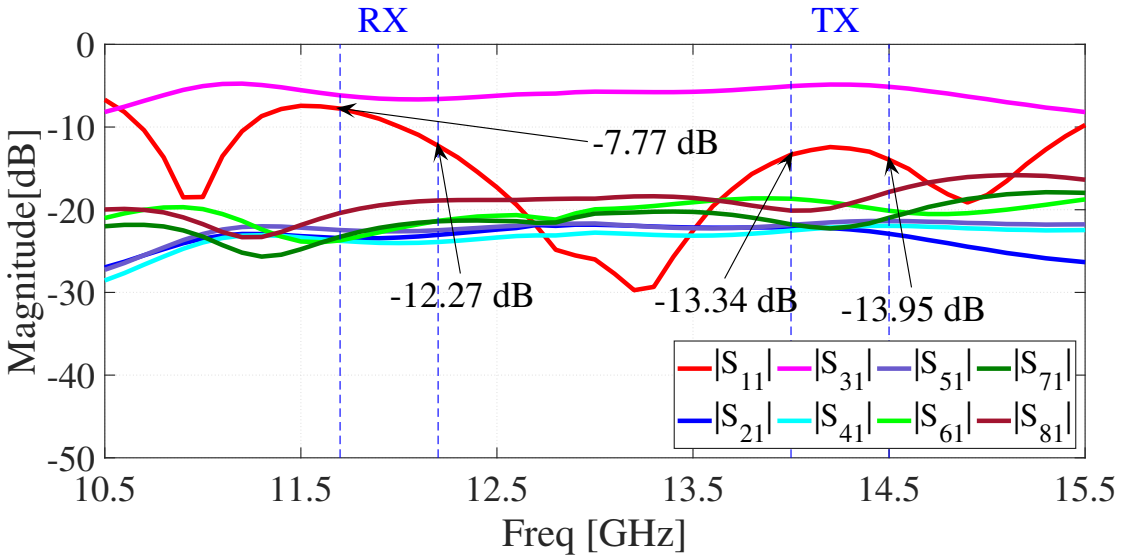


Figure 4.36 – LSSP simulation of the MSA SP16T for port 1 in relation to the others with port 3 ON. Source: Own elaboration.

It is to be expected that the return losses are high for the switched-off ports (Figure 4.38). Return loss from ports 1 and 3 should be lower in this simulation. This was not achieved because the required optimization was not completed.

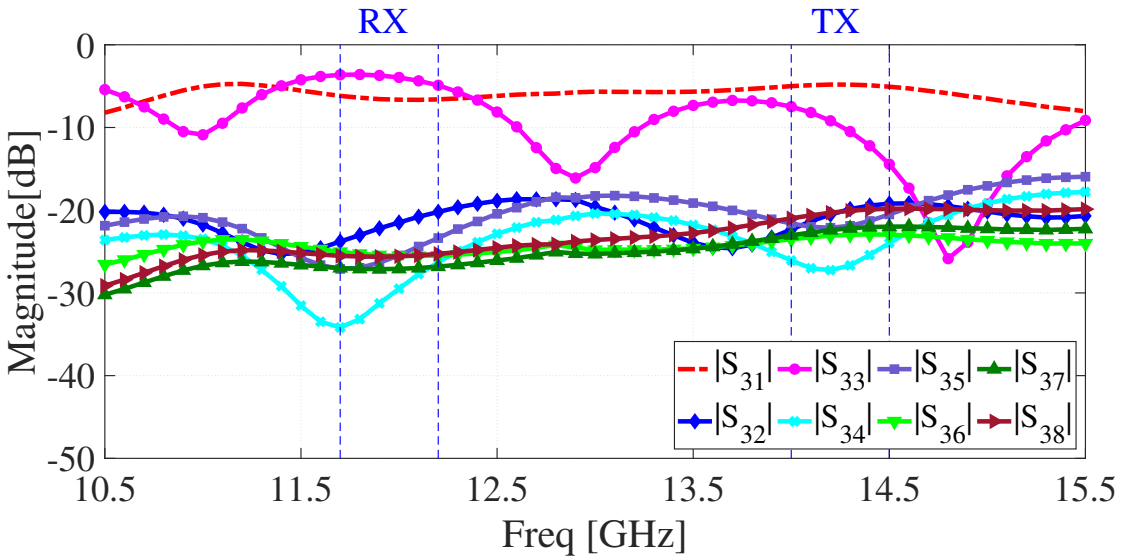


Figure 4.37 – LSSP simulation of the MSA SP16T for port 3 in relation to the others with port 3 ON. Source: Own elaboration

Unfortunately, there were schedule delays and issues with manufacturers and suppliers, so it was impossible to ship to manufacturing in time for the board to return for SP16T switch matrix testing. The analysis of *Yield* was also not done due to the excessive simulation time that demands such a large structure and with many variables.

After some testing, the PIN diode switch circuits were a failure. When using a fully workable, and calibrated Vector Network Analyzer (VNA), the cirscuits showed no difference between what was suppose to be ON and OFF states. Therefore the FET switch was made. In this way, with a minor band, less power handling and a better course of action in biasing a transistor, better results were expected.

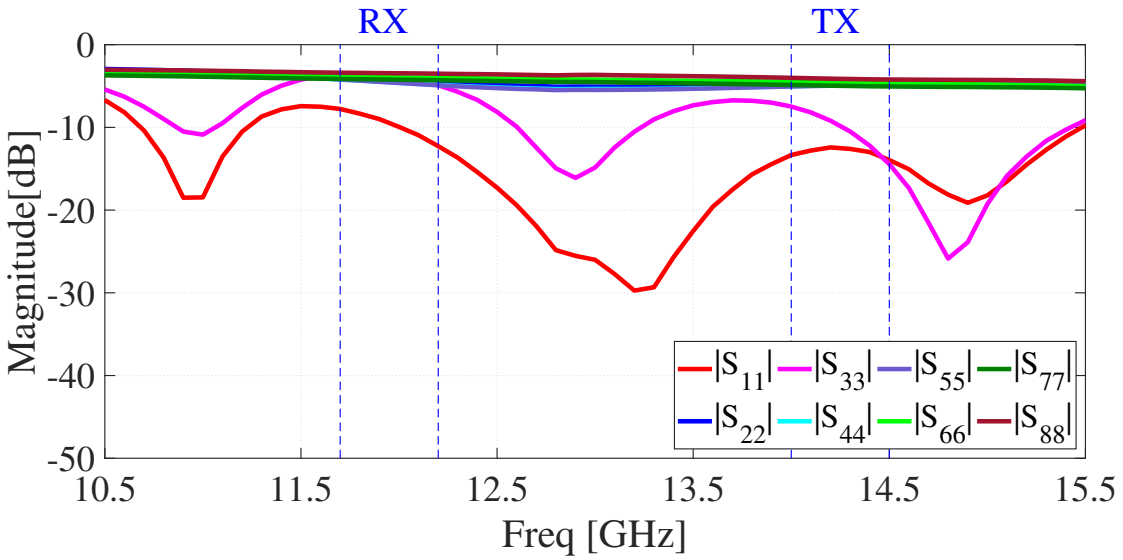


Figure 4.38 – LSSP simulation of the MSA SP16T shows the RL of each port (from 1 to 8) with port 3 ON. Source: Own elaboration.

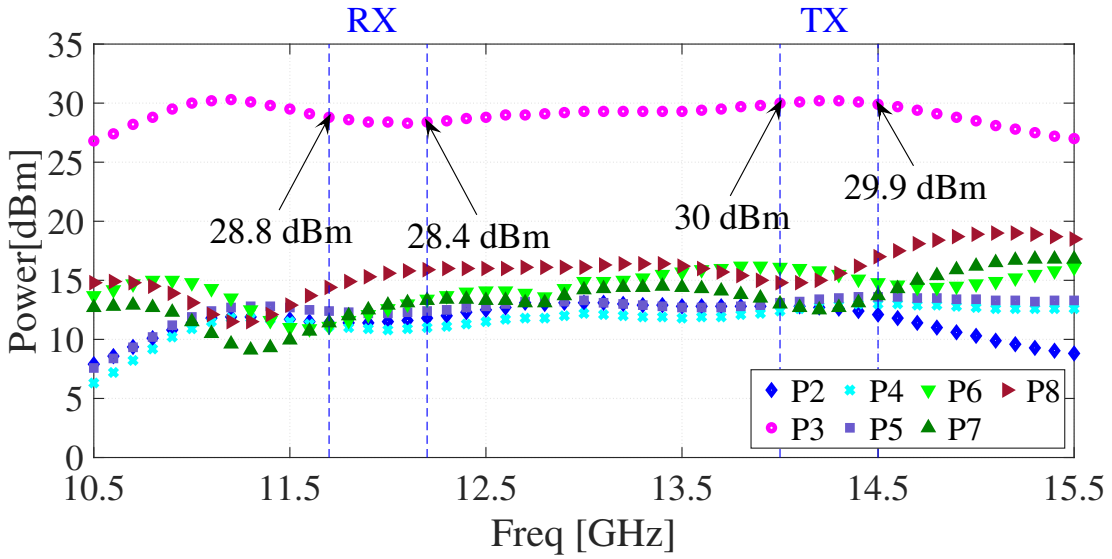


Figure 4.39 – LSSP simulation of the MSA SP16T shows the power coming from ports 2 to 8 for port 3 and port 1 with a source of 35 dBm. Source: Own elaboration.

4.5 FET SWITCH SIMULATION & PROTOTYPE

This section was extracted from Nascimento, Sousa e Rondineau[9]. The designs and simulations were made using ADS from Keysight and its Method of Moment's simulator (MoM). After several design versions and optimizations, the results of the final of the RF SP4T FET switch are presented as follows. One of the most important aspects is the S-parameters simulation, where it is possible to verify if the characteristics of insertion loss, return loss, and isolation are achieved. The insertion loss obtained is below 2.5 dB, and both the return loss and isolation are below -10 dB and -15 dB. These results are presented in Figure 4.40.

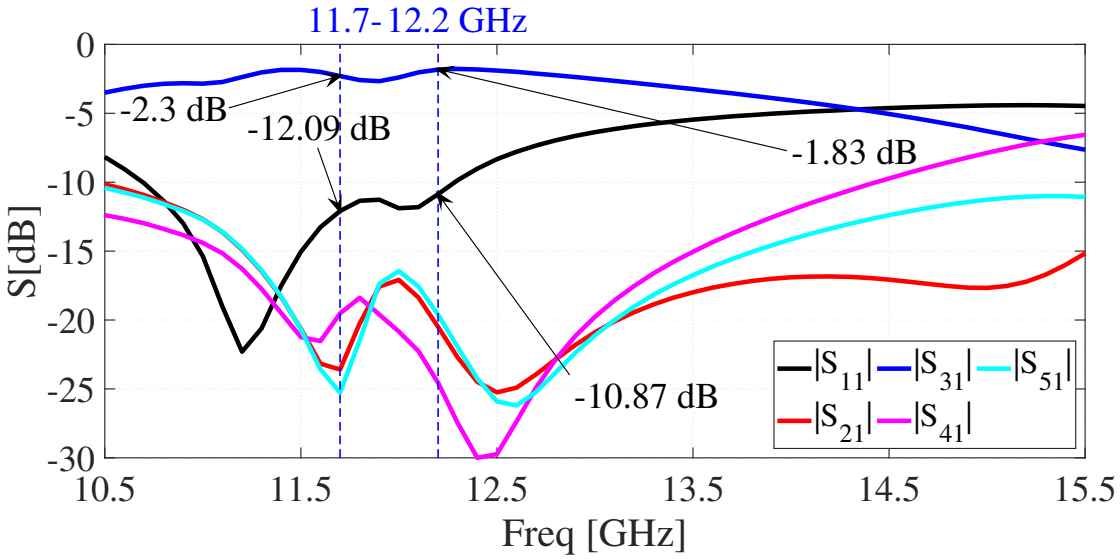


Figure 4.40 – S-parameter simulation performed in ADS Keysight for the RF SP4T FET Switch with the port P3 at ON state, and other ports at OFF state. The insertion loss at the desire band – 11.7 GHz to 12.2 GHz – is considered low (better than 2.5 dB), the return loss is below -10 dB, while the isolation between ports is bigger than 15 dB. All port have similar results. Source: Nascimento, Sousa e Rondineau[9]

Another important specificity of this circuit is the noise added to the signal by the components. the noise should be as low as possible since the radiating system is supposed to receive a low power signal from the satellite (around -110 dB). The next simulation shows the Noise Figure (NF) for each port when only one of them is in the ON state and the rest at OFF state (Figure 4.41). It can be seen that the NF at port P3 is smaller than 2 dB.

From these simulations is possible to verify good results with the achieved insertion loss, return loss, isolation, and noise figure. With that said, the next step was to send the main circuit to be manufactured as a prototype.

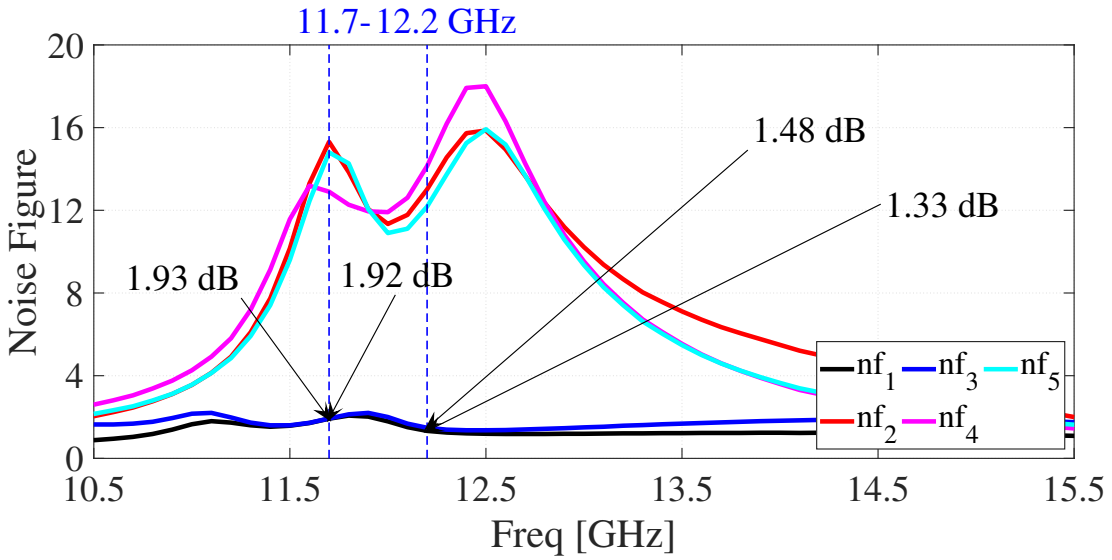


Figure 4.41 – Noise Figure simulation performed in ADS Keysight for the RF SP4T FET Switch with the port P3 at ON state, and other ports at OFF state. The nf_1 and nf_3 for the terminals that are connected (P1 and P3) are smaller than 2 dB at the band. All port have similar results. Source: Nascimento, Sousa e Rondineau[9].

4.5.1 Prototype and tests

After the circuit was sent to fabrication, the components were ordered, and as soon as the transistor arrived, it was tested. Some DC and bias operations were made and verified a procedure for its best function. First applying a $V_{GS} = -1.5$ V, after that, input the $V_{DS} = 2$ V and then adjust the V_{GS} as desired.

There were also made some tests with much smaller frequencies (25 MHz) to check if the JFET was working as expected for the parallel topology commented at the end of Section 2.4, and for the bias points chosen in the previous paragraph. Those tests were made with a function generator at $1\,V_{pp}$, $f = 25$ MHz, $V_{DS} = 0.068$ V, and visualizing it at a spectrum analyzer, and two sources – one for the gate and the other one for the source. At ON state (Figure 4.42) the $V_{GS} = -0.915$ V, $I_{DS} = 0.9$ mA, and output of -5.5 dB.

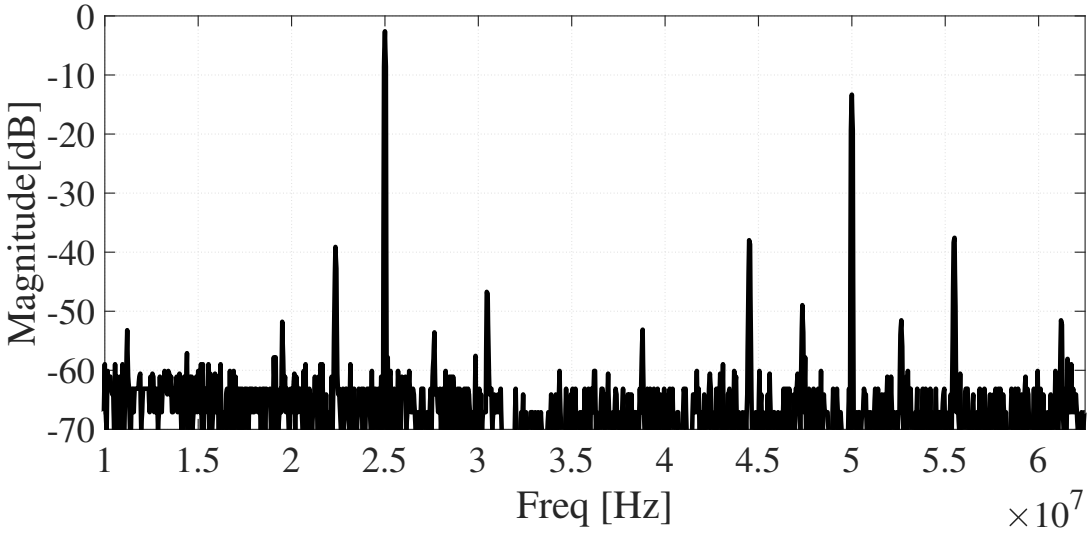


Figure 4.42 – Transistor test at ON state. $1\,\mathrm{V}_{pp}$, $f = 25\,\mathrm{MHz}$, $V_{DS} = 0.068\,\mathrm{V}$, $V_{GS} = -0.915\,\mathrm{V}$, $I_{DS} = 0.9\,\mathrm{mA}$, and output of $-5.5\,\mathrm{dB}$. It is possible to notice the second harmonica at least 10 dB below the first one for the chosen biasing. Source: Nascimento, Sousa e Rondineau[9]

At OFF state (Figure 4.43) the $V_{GS} = 0\,\mathrm{V}$, $I_{DS} = 6.7\,\mathrm{mA}$, and output of $-19.7\,\mathrm{dB}$. A reference without the transistor was taken and the output signal was of $-5.5\,\mathrm{dB}$ for these measurements . Notably, the parallel topology works as expected for lower frequencies, and it is very efficient with almost zero insertion loss and 15 dB of isolation, both at 25 MHz. The harmonics of the signal need to be also taken into consideration ,for future projects, with a much closer look at the spectrum since ,when insulated, they can become bigger than expected.

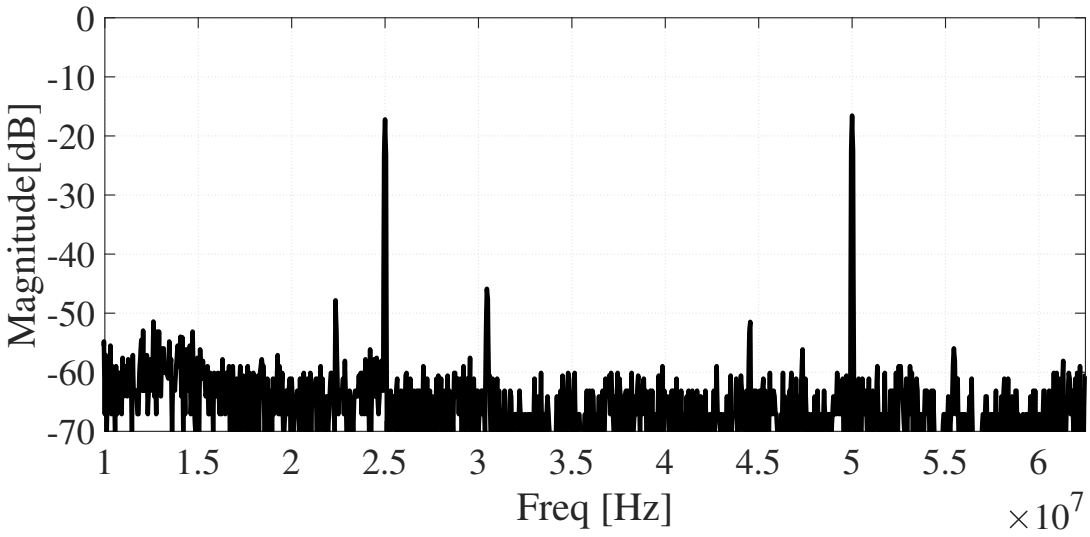


Figure 4.43 – Transistor test at OFF state. $1\,\mathrm{V}_{pp}$, $f = 25\,\mathrm{MHz}$, $V_{DS} = 0.068\,\mathrm{V}$, $V_{GS} = 0\,\mathrm{V}$, $I_{DS} = 6.7\,\mathrm{mA}$, and output of $-19.7\,\mathrm{dB}$ one for the chosen biasing. It is possible to notice the second harmonica a little bit above the first one. Source: Nascimento, Sousa e Rondineau[9]

Later, the PCB arrived and it was verified to confirm that it followed the project and sketches guidelines. The PCB was mounted with the transistors, capacitors, and some other components (Figure 4.44) since there were no problems with it. Unfortunately, it was not possible to test and take measurements of the final circuit at its operation frequency due to the pandemic. The laboratories were closed for an undetermined time with no access to a network analyzer or other types of equipment that can do measurements at Ku-band.

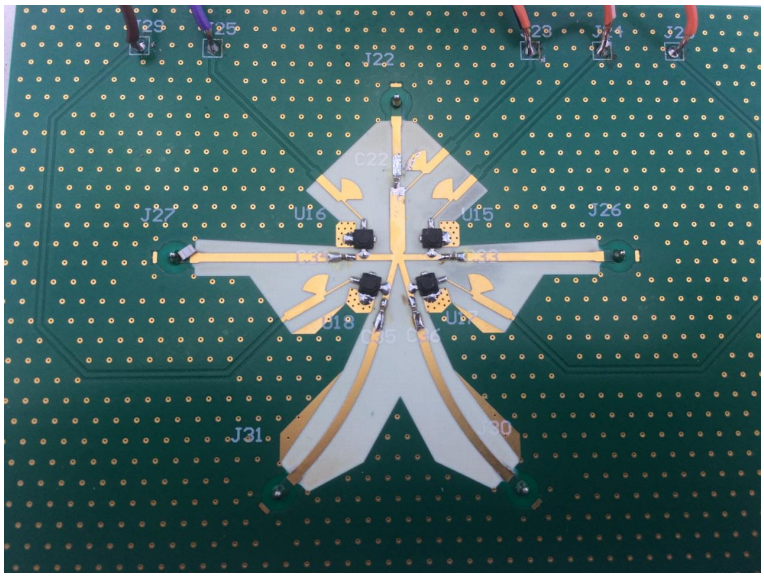


Figure 4.44 – Photo of the fabricated RF SP4T FET switch circuit over a laminate substrate of RO4350B™. Source: Nascimento, Sousa e Rondineau[9].

4.6 ROTMAN LENS & ANALYSIS IN MATLAB

After the simulation of S parameters done previously, the file *.s15p* was imported, converted from amplitude and phase to complex number, and performed an analysis in Matlab to process these data and group them in a way that shows the aiming angles of the created lens intuitively: the Array Factor. The AF (Figure 4.1), adapted from [42], is the sum of the diverse contributions of each element to the perspective of each angle. This makes it possible to analyze the beam's pointing directions.

$$AF(\theta) = \sum_{n=1}^{N} A_n e^{j2\pi(n-1)d\cos\theta}, \tag{4.1}$$

where A_n is the transmission parameter S data from the beam (input) port to the array (output) ports. For Port 1, from S_{81} to S_{151}; for Port 2, from S_{82} to S_{152}; for Port 3, from S_{83} to S_{153}; for Port 4, from S_{84} to S_{154}; for Port 5, from S_{85} to S_{155}; for Port 6, from S_{86} to S_{156}; for Port 7, from S_{87} to S_{157}. N is the number of elements in the array, and d is the distance between elements ($\lambda/2$ @ 11.95 GHz).

As the lens was designed with seven beam ports, it was possible to verify seven aiming angles.

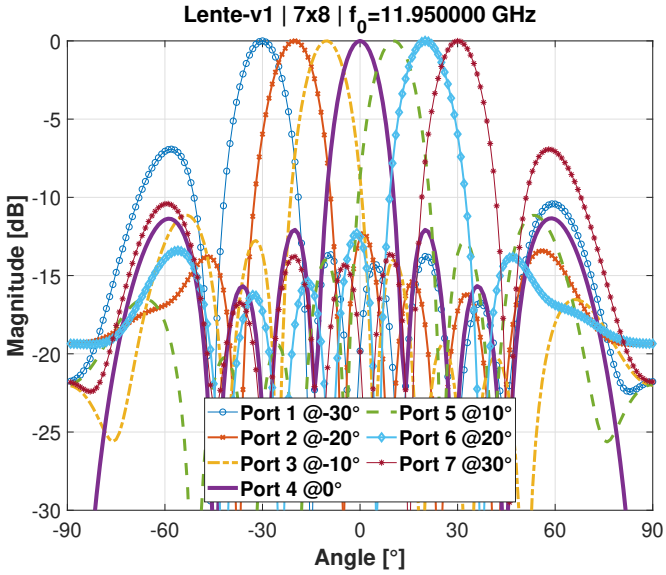


Figure 4.45 – Array factor calculated from Matlab with S parameters @ $\approx$ 11.95 GHz from the 7x8 lens simulation. The results show notes in $-30°$, $-20°$, $-10°$, $0°$, $10°$, $20°$ and $30°$. Source: Own elaboration.

The beams analyzed in Matlab have the expected pointing directions, but the secondary lobes are high, incredibly close to the side beams (-6.92 dB @ $\pm 30°$). This can probably be reversed by optimizing the distance between antennas and improving the side ports for impedance matching.

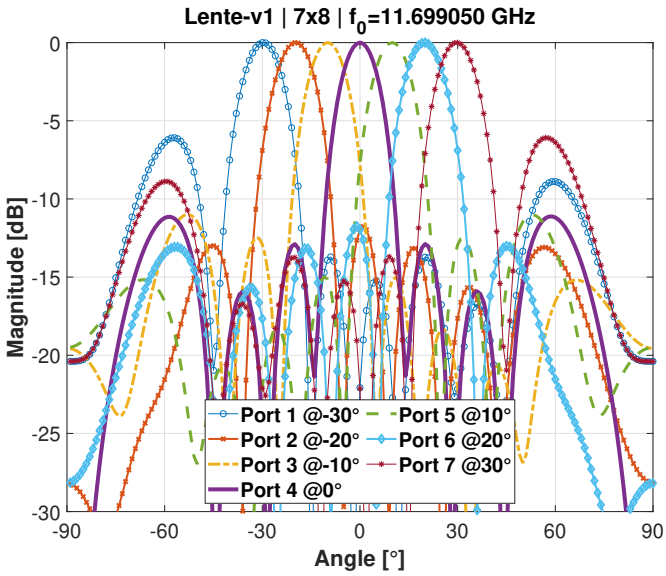


Figure 4.46 – Array factor calculated from Matlab with S parameters @ $\approx 11.70\,\text{GHz}$ from the 7x8 lens simulation. The results show notes in $-30°$, $-20°$, $-10°$, $0°$, $10°$, $20°$ and $30°$. Source: Own elaboration.

For the lower band limit ($\approx 11.70\,\text{GHz}$, Figure 4.46) the pointing angles remain the same as for the central frequency ($\approx 11.95\,\text{GHz}$, Figure 4.45), but the side lobe is larger (($-6.02\,\text{dB}$ @ $\pm 30°$)).

For the upper band limit ($\approx 12.20\,\text{GHz}$, Figure 4.47) the pointing angles remain practically the same as for the central frequency ($\approx 11.95\,\text{GHz}$, Figure 4.45), but with deviation in the Ports 3 and 5 – from $\pm 10°$ to $\pm 11°$ (difference of $1°$). Despite this slight deviation, the sidelobes at $\pm 30°$ are the smallest, with a magnitude of $-7.97\,\text{dB}$.

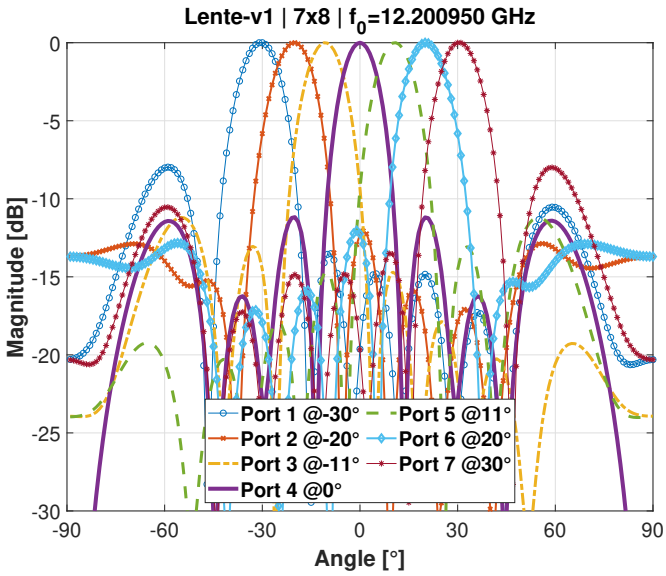


Figure 4.47 – Array factor calculated from Matlab with S parameters @ $\approx 12.20\,\text{GHz}$ from the 7x8 lens simulation. The results show annotations in $-30°$, $-20°$, $-11°$, $0°$, $11°$, $20°$ and $30°$. Source: Own elaboration.

5 DISCUSSION

5.1 FINDINGS

5.1.1 PIN Diode Switch

The PIN diode switch has proven quite challenging to work with. Its design was tricky to get the best of its performance, with numerous optimizations, and its bias is still a question. Nevertheless, it helped to understand planar RF circuits and their features better.

With these designs, it was noticed that space is much more valuable and limiting than before (mainly with the MSA). In addition, inside the limits of fabrication, the manufacturer had many problems. Therefore, it became a good practice to work twice or more the size minimum limit with Brazil's PCB industry. Due to these problems, most circuit tests were postponed for six months.

5.1.2 FET Switch

The RF SP4T FET switch design was a challenge for numerous reasons: higher frequency, short amount of power delivered by the satellite, noise power with levels compared with the signal power, and a possible scale fabrication. These aspects would be impacted by the insertion loss, return loss, insulation, noise figure, size, and processes used to manufacture the switch circuit.

These goals were achieved (at simulation level) by using JFETs with low noise at parallel configuration – one transistor for each one of the four branches – in a microstrip circuit over a substrate in a PCB. Adaptations and optimizations were made to obtain the best grounding at source pads of the JFETs, and better impedance matching at the bias circuits and the main switch circuit. In these simulations, there was acquired an insertion loss of $\approx$2 dB, an return loss lower than 10 dB, and isolation better than 15 dB. The final manufactured circuit is relatively small (26 mm$\times$37 mm), permitting many to be done in only one piece of laminate.

Many DC tests were made, and some procedures were stated for the circuit biasing and correct switching but unluckily, with the pandemic, the RF tests at Ku-band were not made, due to the closed labs and no access to RF equipment capable of measuring the RF SP4T FET switch reliably.

5.1.3 Rotman Lens

Rotman lenses work well for streamlining beamformer designs. This is a simple way to perform the true-time delay typical of these lenses. In this way, it proves to be a valuable tool that can be easily replicated for large-scale production.

The lens developed, and the analysis made in Matlab show that the design of a beamformer using Rotman lenses, RF switches, and antenna array has much potential to work. For this work, a linear array with eight elements and seven pointing angles between $\pm 30°$, with intervals of $10°$ with a center frequency of 11.95 GHz was tried.

During the analysis, it was noticed that the directions for the scan are correct but with the secondary lobes relatively high, mainly in the extreme angles ($30°$ and $-30°$). This may have been due to limitations of the Rotman lens geometry, which provides some internal reflections on the side walls. Improvements can be made to minimize the effects of these sidelobes, such as using more dummy ports, optimizing the distance between antennas, and increasing the array elements. Despite this, the results are pretty satisfactory and show the excellent functioning of the system.

5.2 LIMITATIONS

The main limitations of this project were the fabrication processes of the circuits. Many failures with the manufacturer forced the substrate change many times and compromised the circuit's design.

With the pandemic, many UnB and other laboratories were closed. It affected the design, simulation, prototyping, manufacturing, and DC/RF testing – one of the main points of RF circuits. Due to this, there was a lot of rushed testing and many circuits developed could not be fabricated nor tested.

5.3 RECOMMENDATIONS FOR FUTURE RESEARCH

For future work, the whole system should be studied and assembled. If possible, it should be fabricated outside Brazil and tested with all components in the transceiver (PA, LNA, filters, RF switch, Rotman lenses, and antenna array). It may also be compared with the whole link simulation.

As far as the RF switch is concerned, since there were a few problems with the biasing, an outer bias tee circuit and a proper DC bias circuit should be considered. This can expedite the transition from simulation to testing.

For the Rotman lens, some improvements can be made. In the simulations, some prominent side lobes were noticed, which may affect the lens's whole performance. It can be improved in the final design with more beam ports, better optimization of the dummy ports, and minor scan angles.

5.4 CONCLUSION

The RF switch is essential for the transceiver to function correctly. It is part of the pointing system of the radiating system. Therefore, selecting the beam that must be activated to receive the Ku-band satellite signal is possible.

For the solution of the annotation with the RF switch, market research was carried out about available products and technologies that can be used in the project. In this research, no components were found that would meet the demand for frequency and CW power required by the project, but ways of designing were discovered.

It was decided to design a switch. For this, it must have a low insertion loss to cascade in the future switch matrix and high isolation between channels. Research has shown that reflective switches in parallel have lower insertion loss than others due to impedance matching.

A parallel reflective SPDT microwave switch using two PIN diodes per channel was designed. The PIN diode was used because it has a higher power capacity than other semiconductor devices and low insertion loss in switch designs.

The switch has been developed in different parts: bias tee, diode bias, and the SPDT. All were simulated and optimized separately and together by the method of moments with the help of ADS.

The final SPDT circuit obtained an IL above the maximum requested. This was due to the enormous losses of the created biasing. More important than that was to verify if the developed circuit generates simulations with results close to the tests with the printed circuit.

The developed SPDT circuit was sent for manufacture by a printed circuit board manufacturing company. Unfortunately, the tests were not done because the boards came with defects and quality below expectations, making them impossible. With an analysis of the plates received, one has the impression that the corrosion and copper deposition process was not controlled, with several tracks erased and others shorted. In addition to these, there was also the problem with grounding the connectors.

After the development of the SPDT switch, some versions of SP4T were created, and the one with the best results (SP4T v2.0) was chosen to compose the SP16T matrix. SP4T v2.0

obtained better IL, RL, and ISO values with fewer components (resistors). This is a very relevant evolution concerning SPDT. Its design also proved to be robust to manufacture, achieving reliability above 90%.

The MSA SP16T design had problems with processing power, as its length was higher, required a lot of simulation time, and was frequently broken, so it was not possible to do optimizations and yield analysis. However, insertion loss is low for a 16-port switch despite this high return loss. This makes the SP16T model acceptable for testing with the transceiver, the Rotman lens stack, and the antenna array. Unfortunately all circuits with composed with PIN diodes have failed testing due to inconsistencies in the biasing. The manufacture was questioned about the proper bias for his component but no answer was received.

It was necessary to take a few steps back for a proper switch design. Some changes were made aiming at a less complex circuit. This resulted in a RF FET switch for the downlink with a smaller band, less power handling and the use of field effect transistors. The simulations show good results in terms of insertion loss, return loss, and isolation. A series of biasing test were also made with the transistor and the circuit to define a procedure for actuating in its state. The circuit was fabricated but it was not possible to test it during the pandemic crisis.

The designed Rotman lens showed good results in simulation when evaluating the direction of the beam. This is important because, together with the RF FET switch, it helps to define the beam steering.

In short, much work was done with the design, simulation, optimization, and testing. The FET switch (the one with better results and PCB adjusts and improvements) has good simulation results. This irradiating system, accompanied by the Rotman lens, has shown good simulation results and makes it possible to conduct beam steering and beam forming. More research is needed to test the RF FET switch, Rotman lens design, and both together.

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APPENDIX

A TRANSMISSION LINES

As these are very high frequencies, the use of discrete components (resistors, capacitors, and inductors) is minimal. These often have a physical length longer than the wavelength at the desired frequency. These impedances can be replaced using transmission lines (coaxial cable and microstrip) that consider Maxwell's equations.

In a lossless transmission line, a different impedance Z_{in} is observed as a function of the distance d traveled over it. This impedance can be expressed in terms of the reflection coefficients, for an intrinsic impedance Z_0 as

$$Z_{in}(d) = Z_0 \frac{1 + \Gamma(d)}{1 - \Gamma(d)}. \tag{A.1}$$

Opening the terms Γ as exponentials, and later sines and cosines,

$$Z_{in}(d) = Z_0 \frac{Z_L + jZ_0 \tan(\beta d)}{Z_0 + jZ_L \tan(\beta d)}. \tag{A.2}$$

It is visible that the angle βd interferes with the impedance seen by the load. It is often called **Electrical Length**, being

$$\beta = \frac{2\pi}{\lambda}. \tag{A.3}$$

With that in mind, two tools are widely used for transmission lines: **short circuit terminated** and **open circuit terminated**.

For shorted lines, $Z_L = 0$. One can then simplify the expression A.2 to

$$Z_{in}(d) = jZ_0 \tan(\beta d). \tag{A.4}$$

Putting this equation graphically as a function of the distance d expressed in the Figure by lowercase z.

This shows that, for different electrical lengths, the transmission line ends in a short and can behave as a capacitor or as an inductor, with negative and positive reactances.

The same is true for open circuit terminated transmission lines. For them, Z_L is considered to tend to infinity. Soon,

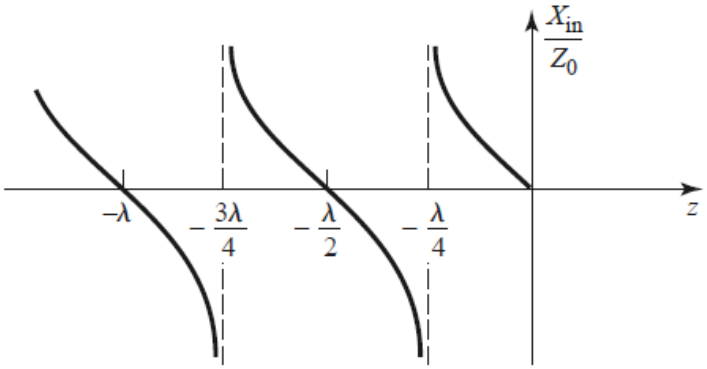


Figure A.1 – Impedance in a shorted-ended transmission line normalized as a function of electrical length. Source: Pozar[5]

$$Z_{in}(d) = -jZ_0\frac{1}{\tan(\beta d)}, \tag{A.5}$$

The same is true for open circuit terminated transmission lines. For them, Z_L is considered to tend to infinity. Soon,

can also be graphed in the same way for a shorted line.

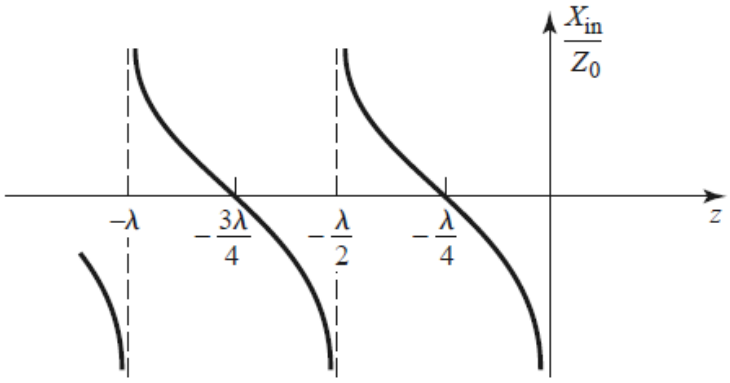
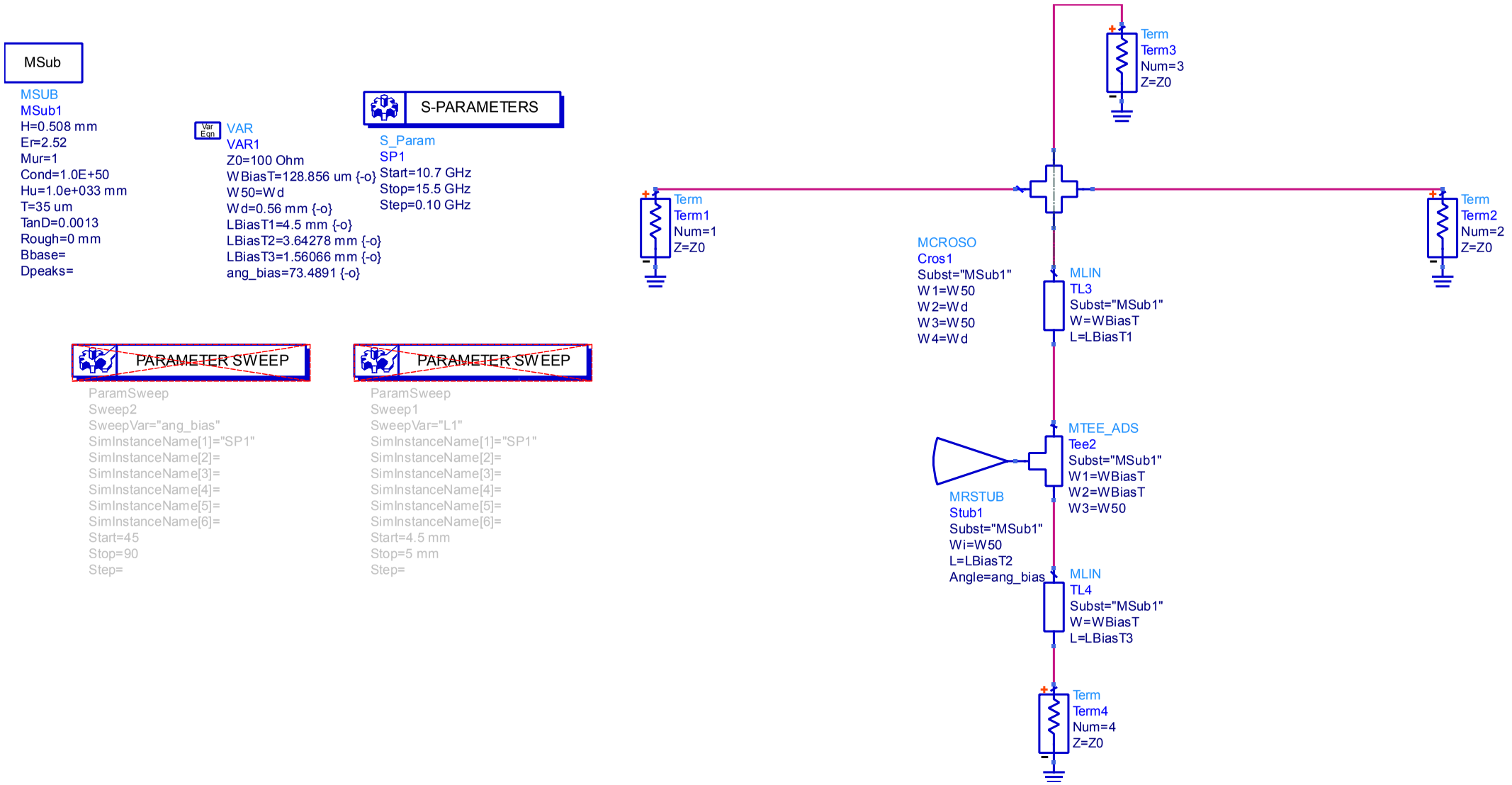


Figure A.2 – Impedance in an open-ended transmission line normalized as a function of electrical length. Source: Pozar[5]

It can be seen that the same thing happens for short-ended lines happens for open-ended lines, only in the “inverse” way. For what would represent capacitances on the shorted lines, now, on the open lines, it represents inductances and vice versa.

B SPDT CIRCUIT SCHEMATICS

B.1 BIAS TEE


MSub
MSUB
MSub1
H=0.508 mm
Er=2.52
Mur=1
Cond=1.0E+50
Hu=1.0e+033 mm
T=35 um
TanD=0.0013
Rough=0 mm
Bbase=
Dpeaks=
VAR
VAR1
Z0=100 Ohm
WBiasT=128.856 um {-o}
W50=Wd
Wd=0.56 mm {-o}
LBiasT1=4.5 mm {-o}
LBiasT2=3.64278 mm {-o}
LBiasT3=1.56066 mm {-o}
ang_bias=73.4891 {-o}
S-PARAMETERS
S_Param
SP1
Start=10.7 GHz
Stop=15.5 GHz
Step=0.10 GHz
PARAMETER SWEEP
ParamSweep
Sweep2
SweepVar="ang_bias"
SimInstanceName[1]="SP1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=45
Stop=90
Step=
PARAMETER SWEEP
ParamSweep
Sweep1
SweepVar="L1"
SimInstanceName[1]="SP1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=4.5 mm
Stop=5 mm
Step=
Term
Term3
Num=3
Z=Z0
Term
Term1
Num=1
Z=Z0
MCROSO
Cros1
Subst="MSub1"
W1=W50
W2=Wd
W3=W50
W4=Wd
Term
Term2
Num=2
Z=Z0
MLIN
TL3
Subst="MSub1"
W=WBiasT
L=LBiasT1
MTEE_ADS
Tee2
Subst="MSub1"
W1=WBiasT
W2=WBiasT
W3=W50
MRSTUB
Stub1
Subst="MSub1"
Wi=W50
L=LBiasT2
Angle=ang_bias
MLIN
TL4
Subst="MSub1"
W=WBiasT
L=LBiasT3
Term
Term4
Num=4
Z=Z0

MSub

MSUB
MSub1
H=0.508 mm
Er=2.52
Mur=1
Cond=1.0E+50
Hu=1.0e+033 mm
T=18 um
TanD=0.0013
Rough=0 mm
Bbase=
Dpeaks=

S-PARAMETERS

S_Param
SP1
Start=10.7 GHz
Stop=15.5 GHz
Step=0.1 GHz

VAR
VAR1
Z0=100 Ohm
w50=0.56 mm
wd=0.56 mm
wbiast=117.136 um {o}
lbiast1=2.70868 mm {o}
lbiast2=3 mm {o}
lbiast3=4.29824 mm {o}
ang=30 {o}

OPTIM

Optim
Optim1
OptimType=Quasi-Newton
MaxIters=300
DesiredError=0.0
StatusLevel=4
FinalAnalysis="None"
NormalizeGoals=yes
SetBestValues=yes
SaveSolns=yes
SaveGoals=yes
SaveOptimVars=no
UpdateDataset=yes
SaveNominal=no
SaveAllIterations=no
UseAllOptVars=yes
UseAllGoals=yes
SaveCurrentEF=no
EnableCockpit=yes
SaveAllTrials=no

S-PARAMETERS

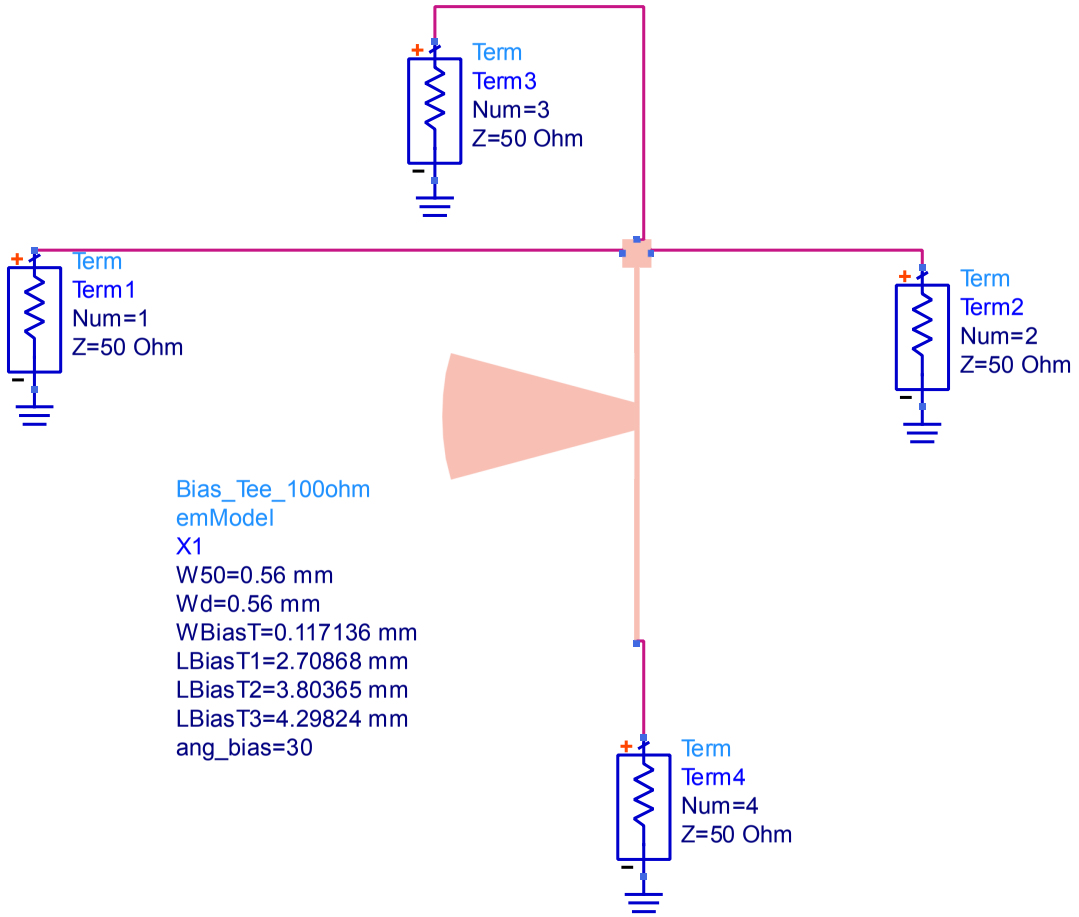
S_Param
SP2
Start=11.2 GHz
Stop=15 GHz
Step=1.9 GHz

GOAL

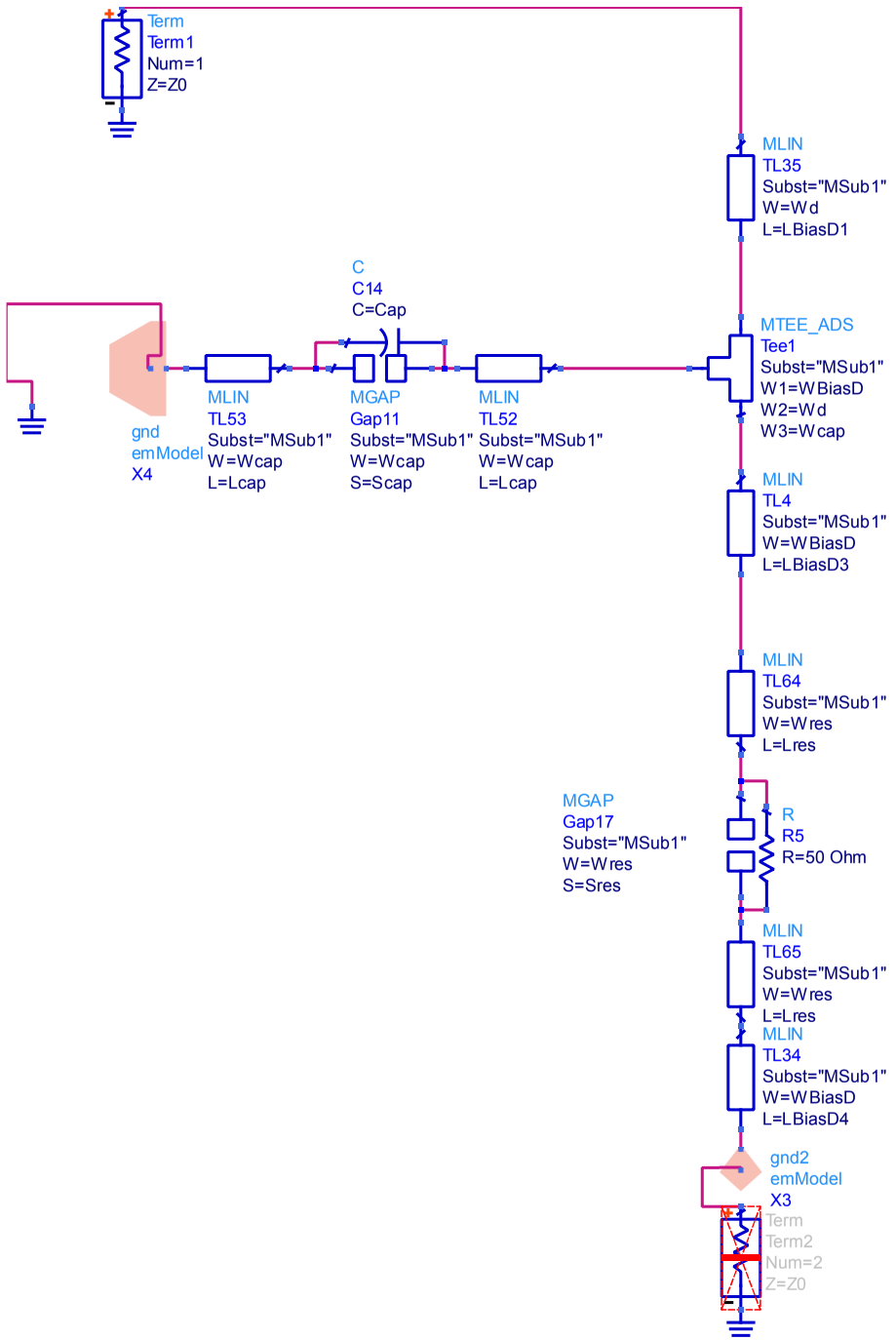
Goal
OptimGoal1
Expr="dB(S(2,1))"
SimInstanceName="SP2"
Weight=1

GOAL

Goal
OptimGoal2
Expr="dB(S(4,1))"
SimInstanceName="SP2"
Weight=1



B.2 DIODE BIAS



MSub

MSUB
MSub1
H=0.508 mm
Er=2.52
Mur=1
Cond=1.0E+50
Hu=1.0e+033 mm
T=35 um
TanD=0.0013
Rough=0 mm
Bbase=
Dpeaks=

S-PARAMETERS

S_Param
SP1
Start=10.7 GHz
Stop=15.5 GHz
Step=0.10 GHz

S-PARAMETERS

S_Param
SP2
Start=11.6 GHz
Stop=14.6 GHz
Step=1.5 GHz

GOAL

Goal
OptimGoal1
Expr="dB(S(1,2))"
SimInstanceName="SP2"
Weight=1

GOAL

Goal
OptimGoal2
Expr="dB(S(1,1))"
SimInstanceName="SP2"
Weight=1

PARAMETER SWEEP

ParamSweep
Sweep2
SweepVar="ang_bias"
SimInstanceName[1]="SP1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=45
Stop=89
Step=

PARAMETER SWEEP

ParamSweep
Sweep1
SweepVar="LBiasD1"
SimInstanceName[1]="SP1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=1 mm
Stop=10 mm
Step=1 mm

PARAMETER SWEEP

ParamSweep
Sweep3
SweepVar="WBias"
SimInstanceName[1]="SP1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=0.1 mm
Stop=0.3 mm
Step=

OPTIM

Optim
Optim1
OptimType=Hybrid
MaxIters=300
DesiredError=0.0
StatusLevel=4
FinalAnalysis="None"
NormalizeGoals=yes
SetBestValues=yes
SaveSolns=yes
SaveGoals=yes
SaveOptimVars=no
UpdateDataset=yes
SaveNominal=no
SaveAllIterations=no
UseAllOptVars=yes
UseAllGoals=yes
SaveCurrentEF=no
EnableCockpit=yes
SaveAllTrials=no

VAR
VAR1
Z0=100 Ohm
Cap=10 nF
coef=0.1
Wres=0.406 mm
Sres=0.3048 mm
Lres=1.016 mm
Wcap=0.610 mm
Scap=0.406 mm
Lcap=1.016 mm
Wd=0.56 mm
WBiasD=0.105 mm
LBiasD1=338.375 um {o}
LBiasD2=200.324 um {o}
LBiasD3=500 um {o}
LBiasD4=500 um {o}

VAR
Variaveis_BiasD
coef=0.8
Z0=100 Ohm
Cap=10 nF
Wres=0.406 mm
Wd=0.56 mm
Sres=0.406mm
Lres=0.305 mm
Wcap=0.610 mm
Scap=0.406 mm
Lcap=0.305 mm
WBiasD=0.105 mm
LBiasD1=300 um {o}
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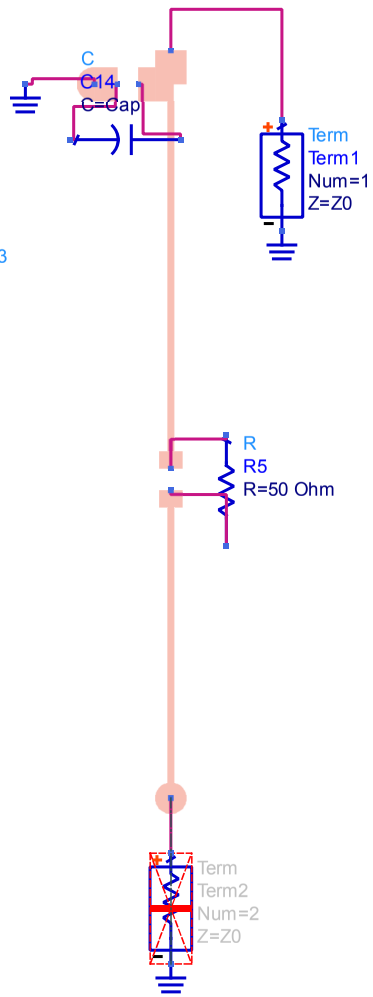
LBiasD3=6.39977 mm {o}
LBiasD4=5.03414 mm {o}



bias_diode_cap_100ohm_v3
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X1
Wres=0.406 mm
Sres=0.406 mm
Lres=0.305 mm
Wd=0.56 mm
Wcap=0.610 mm
Scap=0.406 mm
Lcap=0.305 mm
WBiasD=182.935 um
LBiasD1=LBiasD1
LBiasD2=0.100 mm
LBiasD3=4.39794 mm
LBiasD4=3.62884 mm

MSub

MSUB
MSub1
H=0.508 mm
Er=2.52
Mur=1
Cond=1.0E+50
Hu=1.0e+033 mm
T=35 um
TanD=0.0013
Rough=0 mm
Bbase=
Dpeaks=

S-PARAMETERS

S_Param
SP1
Start=10.7 GHz
Stop=15.5 GHz
Step=0.10 GHz

S-PARAMETERS

S_Param
SP2
Start=11.6 GHz
Stop=14.6 GHz
Step=1.5 GHz

OPTIM

Optim
Optim1
OptimType=Hybrid
MaxIters=300
DesiredError=0.0
StatusLevel=4
FinalAnalysis="None"
NormalizeGoals=yes
SetBestValues=yes
SaveSolns=yes
SaveGoals=yes
SaveOptimVars=no
UpdateDataset=yes
SaveNominal=no
SaveAllIterations=no
UseAllOptVars=yes
UseAllGoals=yes
SaveCurrentEF=no
EnableCockpit=yes
SaveAllTrials=no

PARAMETER SWEEP

ParamSweep
Sweep2
SweepVar="ang_bias"
SimInstanceName[1]="SP1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=45
Stop=89
Step=

PARAMETER SWEEP

ParamSweep
Sweep1
SweepVar="LBiasD1"
SimInstanceName[1]="SP1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=1 mm
Stop=7 mm
Step=1 mm

PARAMETER SWEEP

ParamSweep
Sweep3
SweepVar="WBias"
SimInstanceName[1]="SP1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=0.1 mm
Stop=0.3 mm
Step=

VAR

Variaveis_BiasD
coef=0.8
Z0=100 Ohm
Cap=10 nF
Wres=0.406 mm
Wd=0.56 mm
Sres=0.406mm
Lres=0.305 mm
Wcap=0.610 mm
Scap=0.406 mm
Lcap=0.305 mm
WBiasD=0.105 mm
LBiasD1=300 um {o}
LBiasD2=100.059 um {-o}
LBiasD3=6.39977 mm {o}
LBiasD4=5.03414 mm {o}

VAR

VAR1
Z0=100 Ohm
Cap=10 nF
coef=0.1
Wres=0.406 mm
Sres=0.3048 mm
Lres=1.016 mm
Wcap=0.610 mm
Scap=0.406 mm
Lcap=1.016 mm
Wd=0.56 mm
WBiasD=0.105 mm
LBiasD1=338.375 um {o}
LBiasD2=200.324 um {o}
LBiasD3=500 um {o}
LBiasD4=500 um {o}

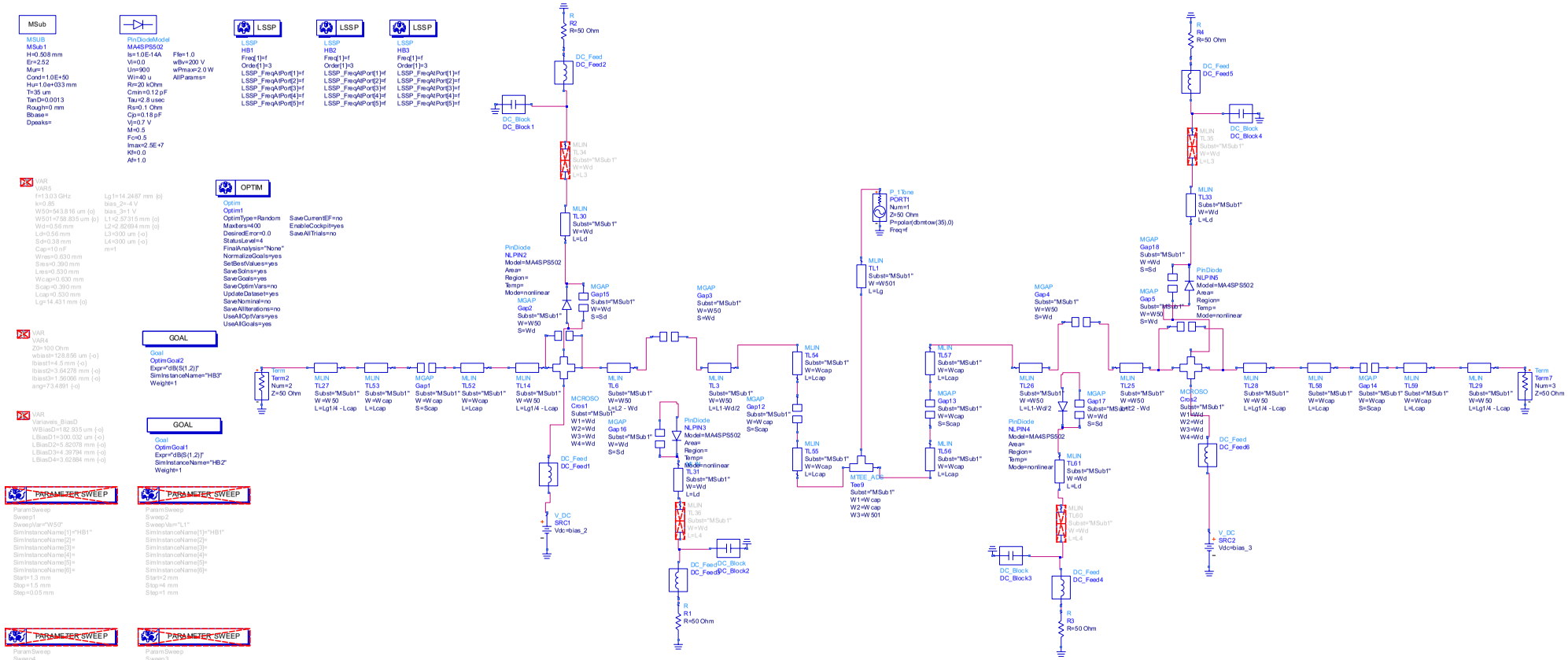
GOAL

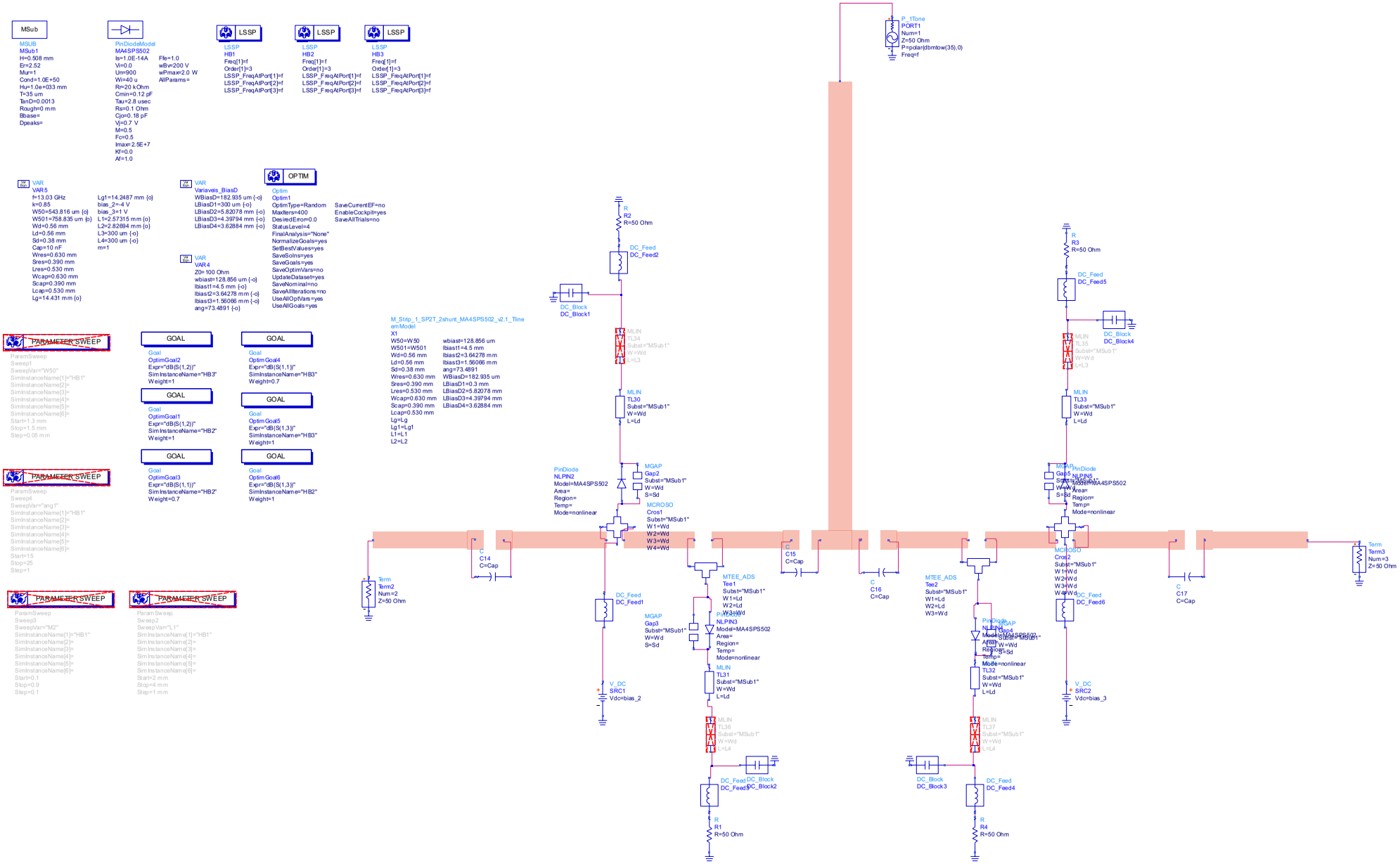
Goal
OptimGoal1
Expr="dB(S(1,2))"
SimInstanceName="SP2"
Weight=1

GOAL

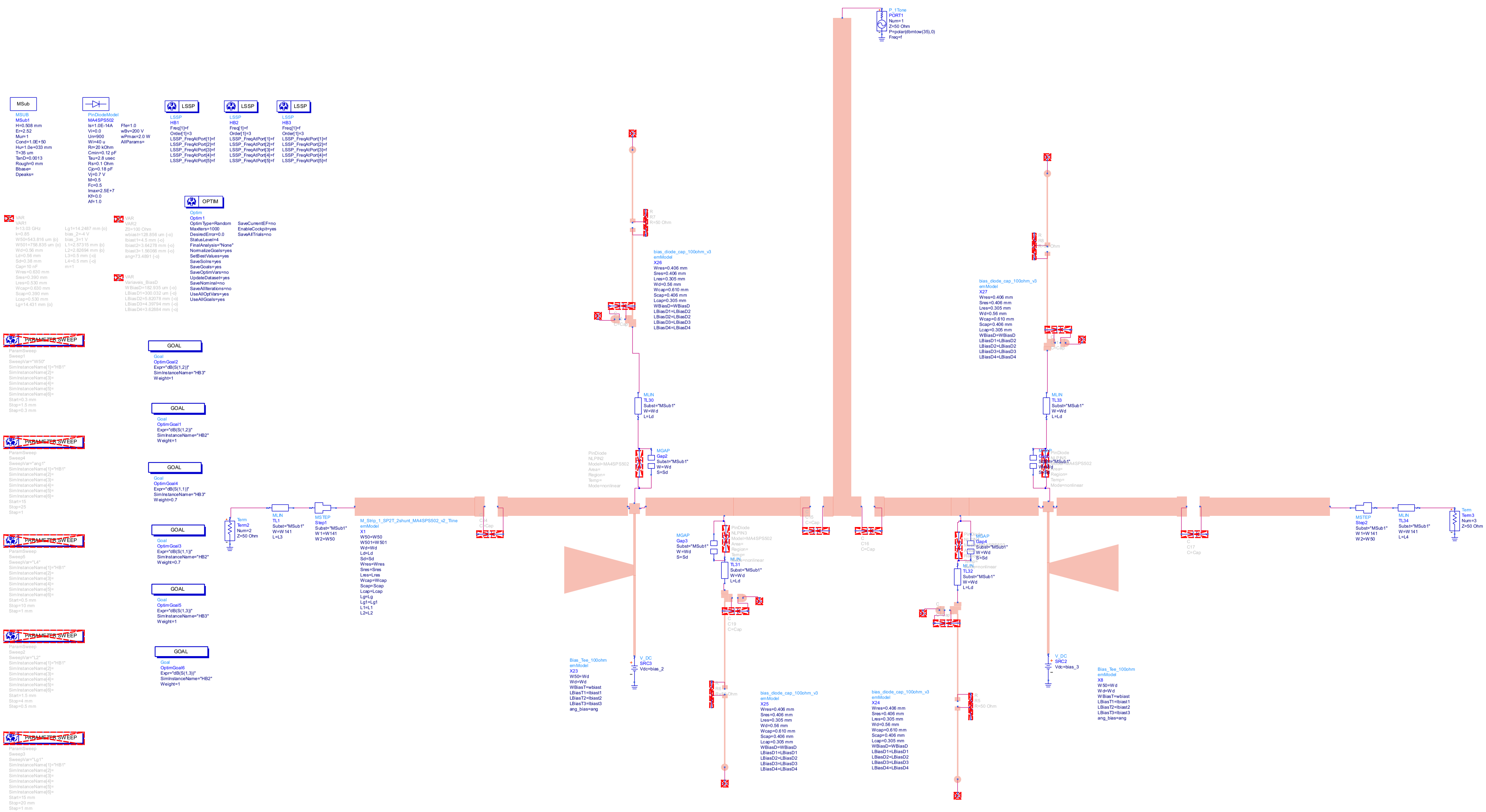
Goal
OptimGoal2
Expr="dB(S(1,1))"
SimInstanceName="SP2"
Weight=1

B.3 SPDT CIRCUIT

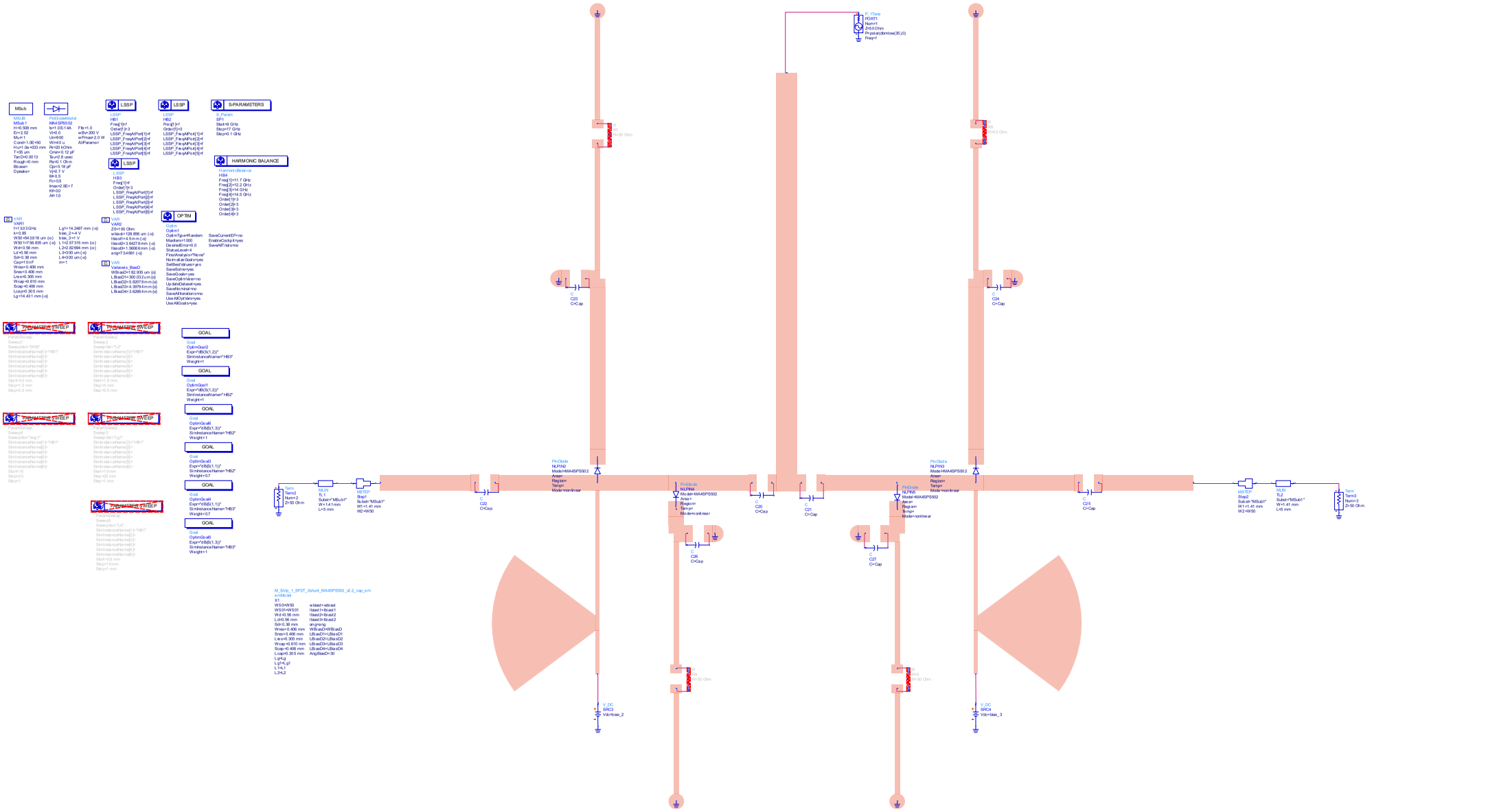

MSub
MSUB
MSub1
H=0.508 mm
Er=2.52
Mur=1
Cond=1.0E+50
Hu=1.0e+033 mm
T=35 um
TanD=0.0013
Rough=0 mm
Bbase=
Dpeaks=
PinDiodeModel
MA4SPS502
Is=1.0E-14A
Vj=0.0
Um=900
W/n=40 u
R=20 kOhm
Cmin=0.12 pF
Tau=2.8 usec
Rs=0.1 Ohm
Cjo=0.18 pF
Vj=0.7 V
M=0.5
Fc=0.5
Imax=2.5E+7
Kf=0.0
Af=1.0
Ffe=1.0
wBv=200 V
wPmax=2.0 W
AllParams=
LSSP
HB1
Freq[1]=f
Order[1]=3
LSSP_FreqAtPort[1]=f
LSSP_FreqAtPort[2]=f
LSSP_FreqAtPort[3]=f
LSSP_FreqAtPort[4]=f
LSSP_FreqAtPort[5]=f
HB2
HB3
VAR
VAR5
f=13.03 GHz
k=0.85
W50=543.816 um {o}
W501=758.835 um {o}
Wd=0.56 mm
Ld=0.56 mm
Sd=0.38 mm
Cap=1.0 nF
Wres=0.630 mm
Sres=0.390 mm
Lres=0.530 mm
Wcap=0.630 mm
Scap=0.390 mm
Lcap=0.530 mm
Lg=14.431 mm {o}
Lg1=14.2487 mm {o}
bias_2=-4 V
bias_3=1 V
L1=2.97315 mm {o}
L2=2.82694 mm {o}
L3=300 um {-o}
L4=300 um {-o}
m=1
OPTIM
Optim
Optim1
OptimType=Random
Maxiters=400
DesiredError=0.0
StatusLevel=4
FinalAnalysis="None"
NormalizeGoals=yes
SetBestValues=yes
SaveSolns=yes
SaveGoals=yes
SaveOptimVars=no
UpdateDatset=yes
SaveNominal=no
SaveAllIterations=no
UseAIOptVars=yes
UseAIGoals=yes
SaveCurrentIEF=no
EnableCockpit=yes
SaveAllTrials=no
VAR
VAR4
Z0=100 Ohm
wbias=128.856 um {-o}
lbias1=4.5 mm {-o}
lbias2=3.64278 mm {-o}
lbias3=1.56066 mm {-o}
ang=73.4891 {-o}
GOAL
Goal
OptimGoal2
Expr="dB(S(1,2))"
SimInstanceName="HB3"
Weight=1
VAR
Variables_BiasD
WBiasD=182.935 um {-o}
LBiasD1=300.032 um {-o}
LBiasD2=5.82078 mm {-o}
LBiasD3=4.39794 mm {-o}
LBiasD4=3.62884 mm {-o}
GOAL
Goal
OptimGoal1
Expr="dB(S(1,2))"
SimInstanceName="HB2"
Weight=1
PARAMETER SWEEP
ParamSweep
Sweep1
SweepVar="W50"
SimInstanceName[1]="HB1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=1.3 mm
Stop=1.5 mm
Step=0.05 mm
Sweep2
SweepVar="L1"
Start=2 mm
Stop=4 mm
Step=1 mm
Sweep4
SweepVar="ang1"
Start=15
Stop=25
Step=1
Sweep3
SweepVar="M2"
Start=0.1
Stop=0.9
Step=0.1
R
R2
R=50 Ohm
DC_Feed
DC_Feed2
DC_Block
DC_Block1
MLIN
TL34
Subst="MSub1"
W=Wd
L=L3
TL30
L=Ld
PinDiode
NLPIN2
Model=MA4SPS502
Area=
Region=
Temp=
Mode=nonlinear
MGAP
Gap2
Subst="MSub1"
W=W50
S=Wd
Gap15
S=Sd
Gap3
Gap1
W=Wcap
S=Scap
Term
Term2
Num=2
Z=50 Ohm
TL27
W=W50
L=Lg1/4 - Lcap
TL53
L=Lcap
TL52
TL14
L=Lg1/4 - Lcap
MCROSO
Cros1
W1=Wd
W2=Wd
W3=Wd
W4=Wd
DC_Feed1
V_DC
SRC1
Vdc=bias_2
TL6
L=L2 - Wd
Gap16
S=Sd
PinDiode
NLPIN3
Model=MA4SPS502
Area=
Region=
Temp=
Mode=nonlinear
TL31
L=Ld
TL36
L=L4
DC_Feed
DC_Feed3
DC_Block
DC_Block2
R
R1
R=50 Ohm
TL3
L=L1-Wd/2
Gap12
TL54
TL55
MTEE_ADS
Tee9
W1=Wcap
W2=Wcap
W3=W501
P_1Tone
PORT1
Num=1
Z=50 Ohm
P=polar(dbmtow(35),0)
Freq=f
TL1
W=W501
L=Lg
TL57
TL56
Gap13
TL26
L=L1-Wd/2
Gap17
W=Wd
S=Sd
PinDiode
NLPIN4
Model=MA4SPS502
Area=
Region=
Temp=
Mode=nonlinear
TL61
L=Ld
TL60
L=L4
DC_Block
DC_Block3
DC_Feed
DC_Feed4
R
R3
R=50 Ohm
Gap4
Gap5
TL25
L=L2 - Wd
R
R4
R=50 Ohm
DC_Feed
DC_Feed5
DC_Block
DC_Block4
TL35
TL33
L=Ld
Gap18
PinDiode
NLPIN5
Model=MA4SPS502
Area=
Region=
Temp=
Mode=nonlinear
MCROSO
Cros2
W1=Wd
W2=Wd
W3=Wd
W4=Wd
DC_Feed
DC_Feed6
V_DC
SRC2
Vdc=bias_3
TL28
L=Lg1/4 - Lcap
TL58
Gap14
TL59
TL29
Term7
Num=3
Z=50 Ohm


MSub
MSUB
MSub1
H=0.508 mm
Er=2.52
Mur=1
Cond=1.0E+50
Hu=1.0e+033 mm
T=35 um
TanD=0.0013
Rough=0 mm
Bbase=
Dpeaks=
PinDiodeModel
MA4SPS502
Is=1.0E-14A
Vi=0.0
Uni=900
Wi=40 u
Rr=20 kOhm
Cmin=0.12 pF
Tau=2.8 usec
Rs=0.1 Ohm
Cjo=0.18 pF
Vj=0.7 V
M=0.5
Fc=0.5
Imax=2.5E+7
Kf=0.0
Af=1.0
Fte=1.0
wBv=200 V
wPmax=2.0 W
AllParams=
LSSP
HB1
Freq[1]=f
Order[1]=3
LSSP_FreqAtPort[1]=f
LSSP_FreqAtPort[2]=f
LSSP_FreqAtPort[3]=f
HB2
Freq[1]=f
Order[1]=3
LSSP_FreqAtPort[1]=f
LSSP_FreqAtPort[2]=f
LSSP_FreqAtPort[3]=f
HB3
Freq[1]=f
Order[1]=3
LSSP_FreqAtPort[1]=f
LSSP_FreqAtPort[2]=f
LSSP_FreqAtPort[3]=f
VAR
VAR5
f=13.03 GHz
k=0.85
W50=543.816 um {o}
W501=758.835 um {o}
Wd=0.56 mm
Ld=0.56 mm
Sd=0.38 mm
Cap=10 nF
Wres=0.630 mm
Sres=0.390 mm
Lres=0.530 mm
Wcap=0.630 mm
Scap=0.390 mm
Lcap=0.530 mm
Lg=14.431 mm {o}
Lg1=14.2487 mm {o}
bias_2=-4 V
bias_3=1 V
L1=2.57315 mm {o}
L2=2.82694 mm {o}
L3=300 um {-o}
L4=300 um {-o}
m=1
VAR
Variavels_BiasD
WBiasD=182.935 um {-o}
LBiasD1=300 um {-o}
LBiasD2=5.82078 mm {-o}
LBiasD3=4.39794 mm {-o}
LBiasD4=3.62884 mm {-o}
VAR
VAR4
Z0=100 Ohm
wbiast=128.856 um {-o}
lbiast1=4.5 mm {-o}
lbiast2=3.64278 mm {-o}
lbiast3=1.56066 mm {-o}
ang=73.4891 {-o}
OPTIM
Optim
Optim1
OptimType=Random
MaxIters=400
DesiredError=0.0
StatusLevel=4
FinalAnalysis="None"
NormalizeGoals=yes
SetBestVsalues=yes
SaveSolns=yes
SaveGoals=yes
SaveOptimVars=no
UpdateDataset=yes
SaveNominal=no
SaveAllIterations=no
UseAllOptVars=yes
UseAllGoals=yes
SaveCurrentEF=no
EnableCockpit=yes
SaveAllTrials=no
PARAMETER SWEEP
ParamSweep
Sweep1
SweepVar="W50"
SimInstanceName[1]="HB1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=1.3 mm
Stop=1.5 mm
Step=0.05 mm
PARAMETER SWEEP
ParamSweep
Sweep4
SweepVar="ang1"
SimInstanceName[1]="HB1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=15
Stop=25
Step=1
PARAMETER SWEEP
ParamSweep
Sweep3
SweepVar="M2"
SimInstanceName[1]="HB1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=0.1
Stop=0.9
Step=0.1
PARAMETER SWEEP
ParamSweep
Sweep2
SweepVar="L1"
SimInstanceName[1]="HB1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=2 mm
Stop=4 mm
Step=1 mm
GOAL
Goal
OptimGoal2
Expr="dB(S(1,2))"
SimInstanceName="HB3"
Weight=1
GOAL
Goal
OptimGoal1
Expr="dB(S(1,2))"
SimInstanceName="HB2"
Weight=1
GOAL
Goal
OptimGoal3
Expr="dB(S(1,1))"
SimInstanceName="HB2"
Weight=0.7
GOAL
Goal
OptimGoal4
Expr="dB(S(1,1))"
SimInstanceName="HB3"
Weight=0.7
GOAL
Goal
OptimGoal5
Expr="dB(S(1,3))"
SimInstanceName="HB3"
Weight=1
GOAL
Goal
OptimGoal6
Expr="dB(S(1,3))"
SimInstanceName="HB2"
Weight=1
M_Stlp_1_SP2T_2shunt_MA4SPS502_v2.1_TlinemModel
X1
W50=W50
W501=W501
Wd=0.56 mm
Ld=0.56 mm
Sd=0.38 mm
Wres=0.630 mm
Sres=0.390 mm
Lres=0.530 mm
Wcap=0.630 mm
Scap=0.390 mm
Lcap=0.530 mm
Lg=Lg
Lg1=Lg1
L1=L1
L2=L2
wbiast=128.856 um
lbiast1=4.5 mm
lbiast2=3.64278 mm
lbiast3=1.56066 mm
ang=73.4891
WBiasD=182.935 um
LBiasD1=0.3 mm
LBiasD2=5.82078 mm
LBiasD3=4.39794 mm
LBiasD4=3.62884 mm
P_1Tone
PORT1
Num=1
Z=50 Ohm
P=polar(dbmtow(35),0)
Freq=f
R
R2
R=50 Ohm
DC_Feed
DC_Feed2
DC_Block
DC_Block1
MLIN
TL34
Subst="MSub1"
W=Wd
L=L3
MLIN
TL30
Subst="MSub1"
W=Wd
L=Ld
PinDiode
NLPIN2
Model=MA4SPS502
Area=
Region=
Temp=
Mode=nonlinear
MGAP
Gap2
Subst="MSub1"
W=Wd
S=Sd
MCROSO
Cros1
Subst="MSub1"
W1=Wd
W2=Wd
W3=Wd
W4=Wd
C
C14
C=Cap
Term
Term2
Num=2
Z=50 Ohm
DC_Feed
DC_Feed1
V_DC
SRC1
Vdc=bias_2
MGAP
Gap3
Subst="MSub1"
W=Wd
S=Sd
MTEE_ADS
Tee1
Subst="MSub1"
W1=Ld
W2=Ld
W3=Wd
PinDiode
NLPIN3
Model=MA4SPS502
Area=
Region=
Temp=
Mode=nonlinear
MLIN
TL31
Subst="MSub1"
W=Wd
L=Ld
MLIN
TL36
Subst="MSub1"
W=Wd
L=L4
DC_Feed
DC_Feed3
DC_Block
DC_Block2
R
R1
R=50 Ohm
C
C15
C=Cap
C
C16
C=Cap
MTEE_ADS
Tee2
Subst="MSub1"
W1=Ld
W2=Ld
W3=Wd
PinDiode
NLPIN4
Model=MA4SPS502
Area=
Region=
Temp=
Mode=nonlinear
MLIN
TL32
Subst="MSub1"
W=Wd
L=Ld
MLIN
TL37
Subst="MSub1"
W=Wd
L=L4
DC_Block
DC_Block3
DC_Feed
DC_Feed4
R
R4
R=50 Ohm
R
R3
R=50 Ohm
DC_Feed
DC_Feed5
DC_Block
DC_Block4
MLIN
TL35
Subst="MSub1"
W=Wd
L=L3
MLIN
TL33
Subst="MSub1"
W=Wd
L=Ld
MCROSO
Cros2
Subst="MSub1"
W1=Wd
W2=Wd
W3=Wd
W4=Wd
DC_Feed
DC_Feed6
V_DC
SRC2
Vdc=bias_3
C
C17
C=Cap
Term
Term3
Num=3
Z=50 Ohm

B.4 COMPLETE SPDT CIRCUIT



P_1Tone
PORT1
Num=1
Z=50 Ohm
P=polar(dbmtow(35),0)
Freq=f
MSub
MSUB
MSub1
H=0.508 mm
Er=2.52
Mur=1
Cond=1.0E+50
Hu=1.0e+033 mm
T=35 um
TanD=0.0013
Rough=0 mm
Bbase=
Dpeaks=
PinDiodeModel
MA4SPS502
Is=1.0E-14A
Vi=0.0
Un=900
Wi=40 u
Rr=20 kOhm
Cmin=0.12 pF
Tau=2.8 usec
Rs=0.1 Ohm
Cjo=0.18 pF
Vj=0.7 V
M=0.5
Fc=0.5
Imax=2.5E+7
Kf=0.0
Af=1.0
Ffe=1.0
wBv=200 V
wPmax=2.0 W
AllParams=
LSSP
HB1
Freq[1]=f
Order[1]=3
LSSP_FreqAtPort[1]=f
LSSP_FreqAtPort[2]=f
LSSP_FreqAtPort[3]=f
LSSP_FreqAtPort[4]=f
LSSP_FreqAtPort[5]=f
LSSP
HB2
Freq[1]=f
Order[1]=3
LSSP_FreqAtPort[1]=f
LSSP_FreqAtPort[2]=f
LSSP_FreqAtPort[3]=f
LSSP_FreqAtPort[4]=f
LSSP_FreqAtPort[5]=f
LSSP
HB3
Freq[1]=f
Order[1]=3
LSSP_FreqAtPort[1]=f
LSSP_FreqAtPort[2]=f
LSSP_FreqAtPort[3]=f
LSSP_FreqAtPort[4]=f
LSSP_FreqAtPort[5]=f
VAR
VAR1
f=13.03 GHz
k=0.85
W50=543.816 um {o}
W501=758.835 um {o}
Wd=0.56 mm
Ld=0.56 mm
Sd=0.38 mm
Cap=10 nF
Wres=0.630 mm
Sres=0.390 mm
Lres=0.530 mm
Wcap=0.630 mm
Scap=0.390 mm
Lcap=0.530 mm
Lg=14.431 mm {o}
Lg1=14.2487 mm {o}
bias_2=-4 V
bias_3=1 V
L1=2.57315 mm {o}
L2=2.82694 mm {o}
L3=0.5 mm {-o}
L4=0.5 mm {-o}
m=1
VAR
VAR2
Z0=100 Ohm
wbiast=128.856 um {-o}
lbiast1=4.5 mm {-o}
lbiast2=3.64278 mm {-o}
lbiast3=1.56066 mm {-o}
ang=73.4891 {-o}
VAR
Variaveis_BiasD
WBiasD=182.935 um {-o}
LBiasD1=300.032 um {-o}
LBiasD2=5.82078 mm {-o}
LBiasD3=4.39794 mm {-o}
LBiasD4=3.62884 mm {-o}
OPTIM
Optim
Optim1
OptimType=Random
MaxIters=1000
DesiredError=0.0
StatusLevel=4
FinalAnalysis="None"
NormalizeGoals=yes
SetBestValues=yes
SaveSolns=yes
SaveGoals=yes
SaveOptimVars=no
UpdateDataset=yes
SaveNominal=no
SaveAllIterations=no
UseAllOptVars=yes
UseAllGoals=yes
SaveCurrentEF=no
EnableCockpit=yes
SaveAllTrials=no
PARAMETER SWEEP
ParamSweep
Sweep1
SweepVar="W50"
SimInstanceName[1]="HB1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=0.3 mm
Stop=1.5 mm
Step=0.3 mm
PARAMETER SWEEP
ParamSweep
Sweep4
SweepVar="ang1"
SimInstanceName[1]="HB1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=15
Stop=25
Step=1
PARAMETER SWEEP
ParamSweep
Sweep5
SweepVar="L4"
SimInstanceName[1]="HB1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=0.5 mm
Stop=10 mm
Step=1 mm
PARAMETER SWEEP
ParamSweep
Sweep2
SweepVar="L2"
SimInstanceName[1]="HB1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=1.5 mm
Stop=4 mm
Step=0.5 mm
PARAMETER SWEEP
ParamSweep
Sweep3
SweepVar="Lg1"
SimInstanceName[1]="HB1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=15 mm
Stop=20 mm
Step=1 mm
GOAL
Goal
OptimGoal2
Expr="dB(S(1,2))"
SimInstanceName="HB3"
Weight=1
GOAL
Goal
OptimGoal1
Expr="dB(S(1,2))"
SimInstanceName="HB2"
Weight=1
GOAL
Goal
OptimGoal4
Expr="dB(S(1,1))"
SimInstanceName="HB3"
Weight=0.7
GOAL
Goal
OptimGoal3
Expr="dB(S(1,1))"
SimInstanceName="HB2"
Weight=0.7
GOAL
Goal
OptimGoal5
Expr="dB(S(1,3))"
SimInstanceName="HB3"
Weight=1
GOAL
Goal
OptimGoal6
Expr="dB(S(1,3))"
SimInstanceName="HB2"
Weight=1
Term
Term2
Num=2
Z=50 Ohm
MLIN
TL1
Subst="MSub1"
W=W141
L=L3
MSTEP
Step1
Subst="MSub1"
W1=W141
W2=W50
M_Strip_1_SP2T_2shunt_MA4SPS502_v2_Tline
emModel
X1
W50=W50
W501=W501
Wd=Wd
Ld=Ld
Sd=Sd
Wres=Wres
Sres=Sres
Lres=Lres
Wcap=Wcap
Scap=Scap
Lcap=Lcap
Lg=Lg
Lg1=Lg1
L1=L1
L2=L2
C
C14
C=Cap
R
R7
R=50 Ohm
bias_diode_cap_100ohm_v3
emModel
X26
Wres=0.406 mm
Sres=0.406 mm
Lres=0.305 mm
Wd=0.56 mm
Wcap=0.610 mm
Scap=0.406 mm
Lcap=0.305 mm
WBiasD=WBiasD
LBiasD1=LBiasD2
LBiasD2=LBiasD2
LBiasD3=LBiasD3
LBiasD4=LBiasD4
MLIN
TL30
Subst="MSub1"
W=Wd
L=Ld
PinDiode
NLPIN2
Model=MA4SPS502
Area=
Region=
Temp=
Mode=nonlinear
MGAP
Gap2
Subst="MSub1"
W=Wd
S=Sd
Bias_Tee_100ohm
emModel
X23
W50=Wd
Wd=Wd
WBiasT=wbiast
LBiasT1=lbiast1
LBiasT2=lbiast2
LBiasT3=lbiast3
ang_bias=ang
V_DC
SRC3
Vdc=bias_2
MGAP
Gap3
Subst="MSub1"
W=Wd
S=Sd
PinDiode
NLPIN3
Model=MA4SPS502
Area=
Region=
Temp=
Mode=nonlinear
MLIN
TL31
Subst="MSub1"
W=Wd
L=Ld
C
C19
C=Cap
R
R6
R=50 Ohm
bias_diode_cap_100ohm_v3
emModel
X25
Wres=0.406 mm
Sres=0.406 mm
Lres=0.305 mm
Wd=0.56 mm
Wcap=0.610 mm
Scap=0.406 mm
Lcap=0.305 mm
WBiasD=WBiasD
LBiasD1=LBiasD1
LBiasD2=LBiasD2
LBiasD3=LBiasD3
LBiasD4=LBiasD4
C
C15
C=Cap
C
C16
C=Cap
MGAP
Gap4
Subst="MSub1"
W=Wd
S=Sd
MLIN
TL32
Subst="MSub1"
W=Wd
L=Ld
R
R5
R=50 Ohm
bias_diode_cap_100ohm_v3
emModel
X24
Wres=0.406 mm
Sres=0.406 mm
Lres=0.305 mm
Wd=0.56 mm
Wcap=0.610 mm
Scap=0.406 mm
Lcap=0.305 mm
WBiasD=WBiasD
LBiasD1=LBiasD1
LBiasD2=LBiasD2
LBiasD3=LBiasD3
LBiasD4=LBiasD4
R
R8
R=50 Ohm
bias_diode_cap_100ohm_v3
emModel
X27
Wres=0.406 mm
Sres=0.406 mm
Lres=0.305 mm
Wd=0.56 mm
Wcap=0.610 mm
Scap=0.406 mm
Lcap=0.305 mm
WBiasD=WBiasD
LBiasD1=LBiasD2
LBiasD2=LBiasD2
LBiasD3=LBiasD3
LBiasD4=LBiasD4
MLIN
TL33
Subst="MSub1"
W=Wd
L=Ld
PinDiode
NLPIN5
Model=MA4SPS502
Area=
Region=
Temp=
Mode=nonlinear
MGAP
Gap5
Subst="MSub1"
W=Wd
S=Sd
V_DC
SRC2
Vdc=bias_3
Bias_Tee_100ohm
emModel
X8
W50=Wd
Wd=Wd
WBiasT=wbiast
LBiasT1=lbiast1
LBiasT2=lbiast2
LBiasT3=lbiast3
ang_bias=ang
C
C17
C=Cap
MSTEP
Step2
Subst="MSub1"
W1=W141
W2=W50
MLIN
TL34
Subst="MSub1"
W=W141
L=L4
Term
Term3
Num=3
Z=50 Ohm


MSub
PinDiodeModel
LSSP
LSSP
LSSP
S-PARAMETERS
HARMONIC BALANCE
OPTIM
VAR
VAR
VAR
VAR
DataVarSweep
DataVarSweep
DataVarSweep
DataVarSweep
DataVarSweep
DataVarSweep
GOAL
GOAL
GOAL
GOAL
GOAL
GOAL
P_1Tone
R
R
C
C
C
C
C
C
C
C
C
Pin Diode
Pin Diode
Pin Diode
MLIN
MSTEP
MSTEP
MLIN
Term
Term
Term
V_DC
V_DC
M_Strip_1_SP2T_2shunt_MA4SPS502_sl_2_cap_emmMod
X1
W50=W50
W50=W501
Wd=0.56 mm
L=0.56 mm
Sd=0.38 mm
Wsss=0.406 mm
Sss=0.406 mm
Lss=0.305 mm
Wcap=0.610 mm
Scap=0.406 mm
L_cap=0.305 mm
L_g=L_g
L_g1=L_g1
L_1=L_1
L_2=L_2
wbias=wbias1
lbias1=lbias1
lbias2=lbias2
lbias3=lbias2
ang=ang
WBiasD=WBiasD
LBiasD1=LBiasD1
LBiasD2=LBiasD2
LBiasD3=LBiasD3
LBiasD4=LBiasD4
AngBiasD=30

C SP4T CIRCUITS

C.1 SP4T VERSION 1.0

These are the simulations and the *layout* of the first version of the one to four-port switch developed during the project. This version was unsatisfactory, as ports 2 and 5 have very different insertion losses than those simulated in ports 3 and 4.

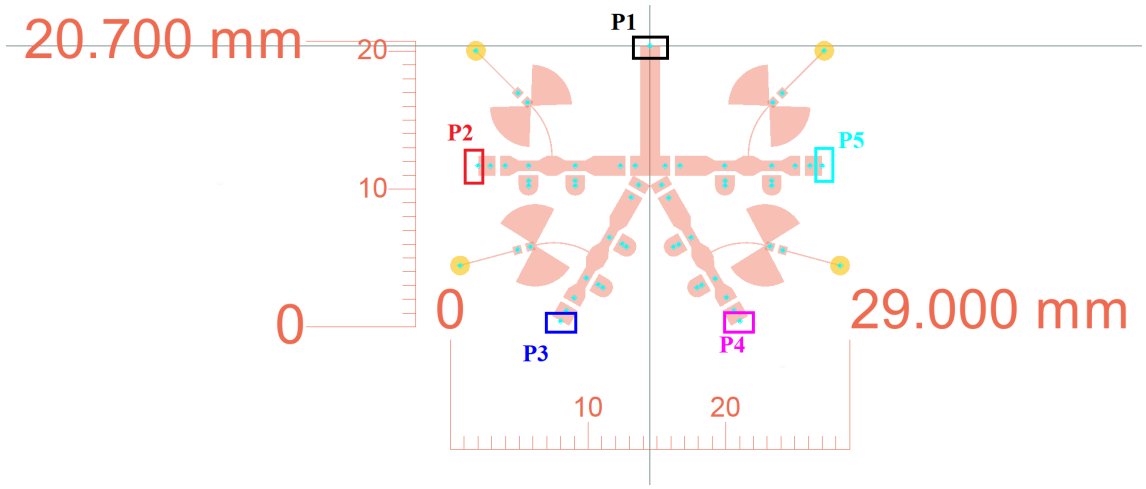


Figure C.1 – SP4T circuit in its first version, showing ports P1 to P5. Source: Own elaboration.

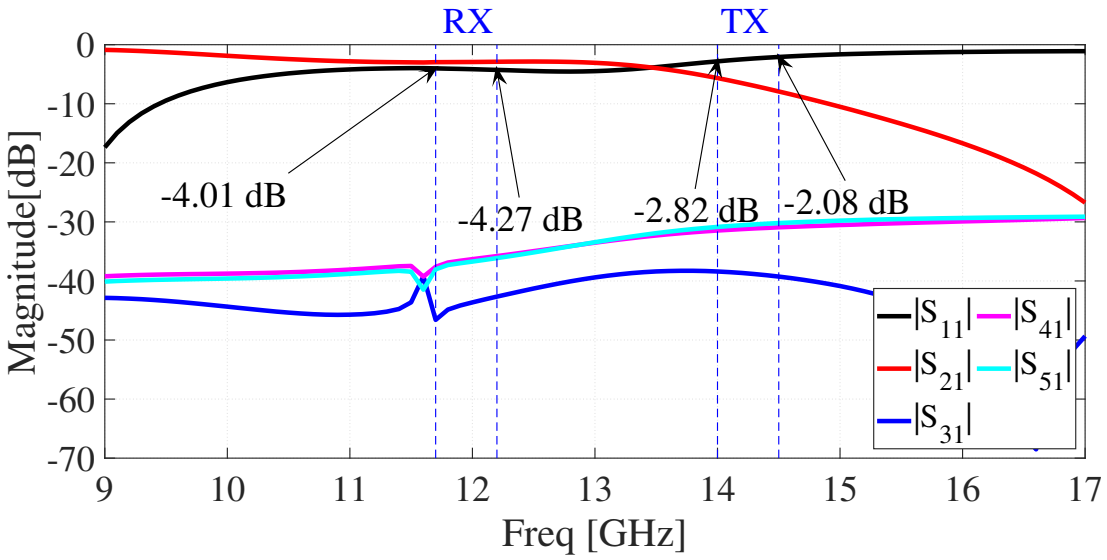


Figure C.2 – LSSP (magnitude in dB) simulation for SP4T v1.0 circuit with projected bias. Port 1 is the source of the RF signal, and port 2 is connected to pass the RF signal. Source: Own elaboration.

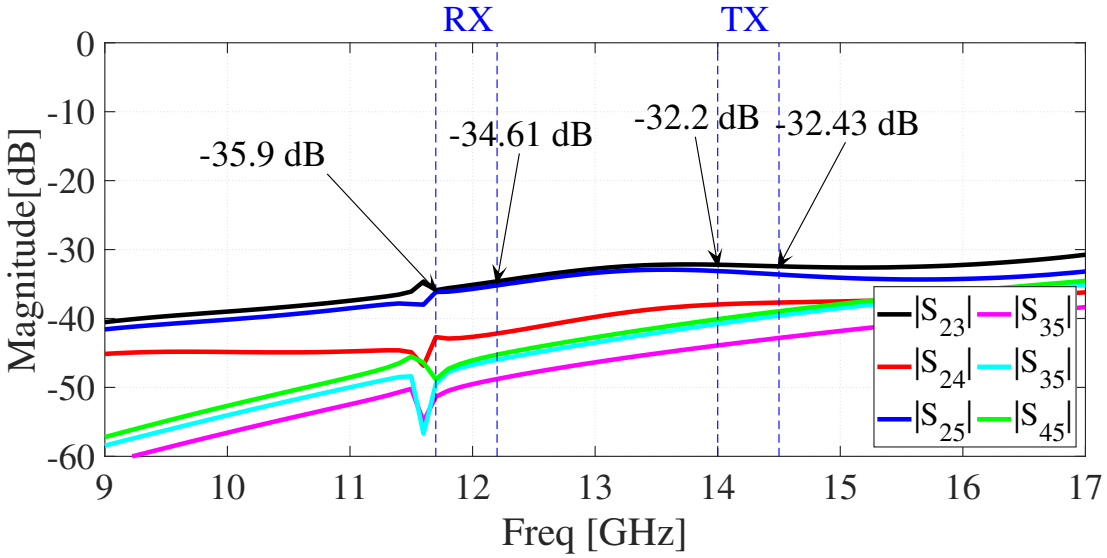


Figure C.3 – LSSP (dB magnitude) simulation for SP4T v1.0 circuit showing isolation between channels. Port 1 is the source of the RF signal, and port 2 is connected to pass the RF signal. Source: Own elaboration.

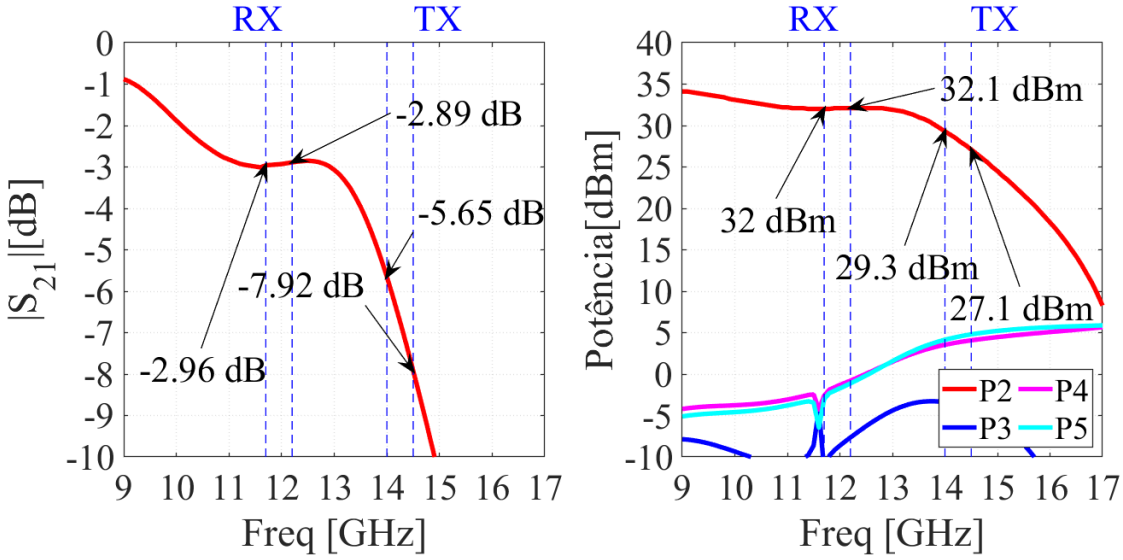


Figure C.4 – LSSP simulation (dB magnitude) for SP4T v1.0 circuit. S_21 on the left, and the power distribution across all ports on the right. Port 1 is the source of the RF signal with a power of 35dBm, and port 2 is connected for the passage of the RF signal. Source: Own elaboration.

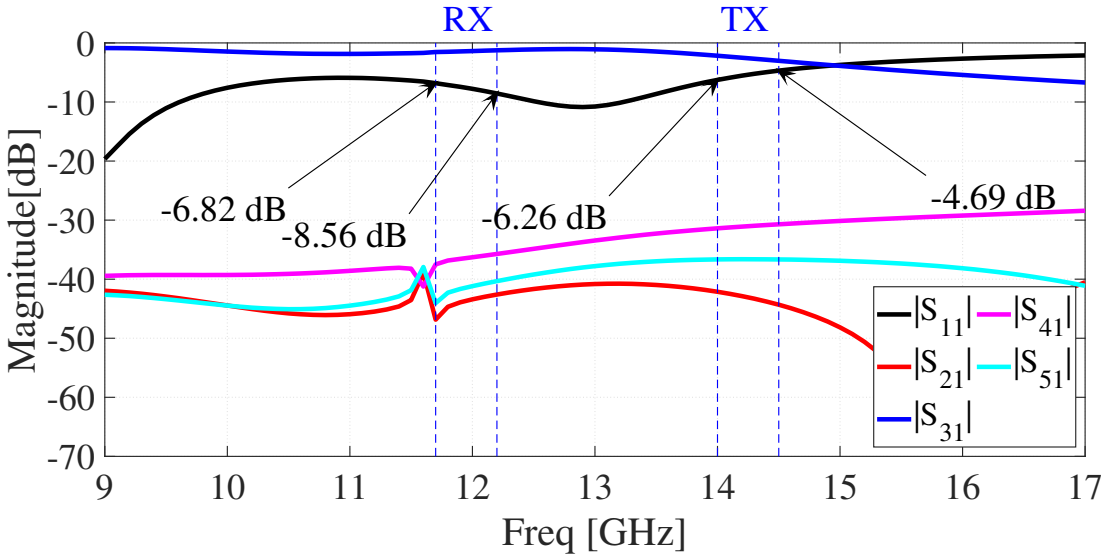


Figure C.5 – LSSP (magnitude in dB) simulation for SP4T v1.0 circuit with projected bias. Port 1 is the source of the RF signal, and port 3 is connected for the passage of the RF signal. Source: Own elaboration.

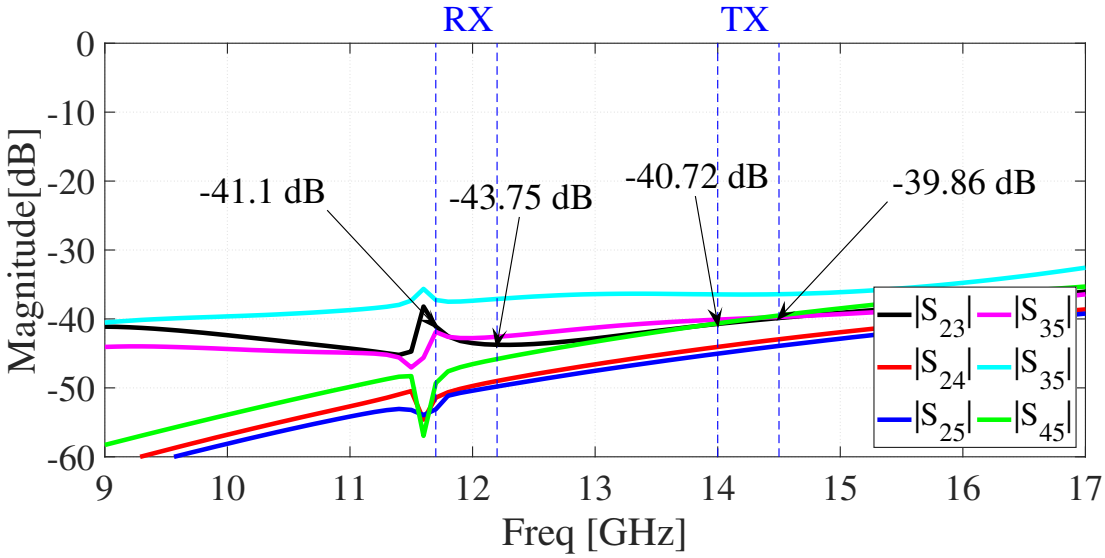


Figure C.6 – LSSP (dB magnitude) simulation for SP4T v1.0 circuit showing isolation between channels. Port 1 is the source of the RF signal, and port 3 is connected for the passage of the RF signal. Source: Own elaboration.

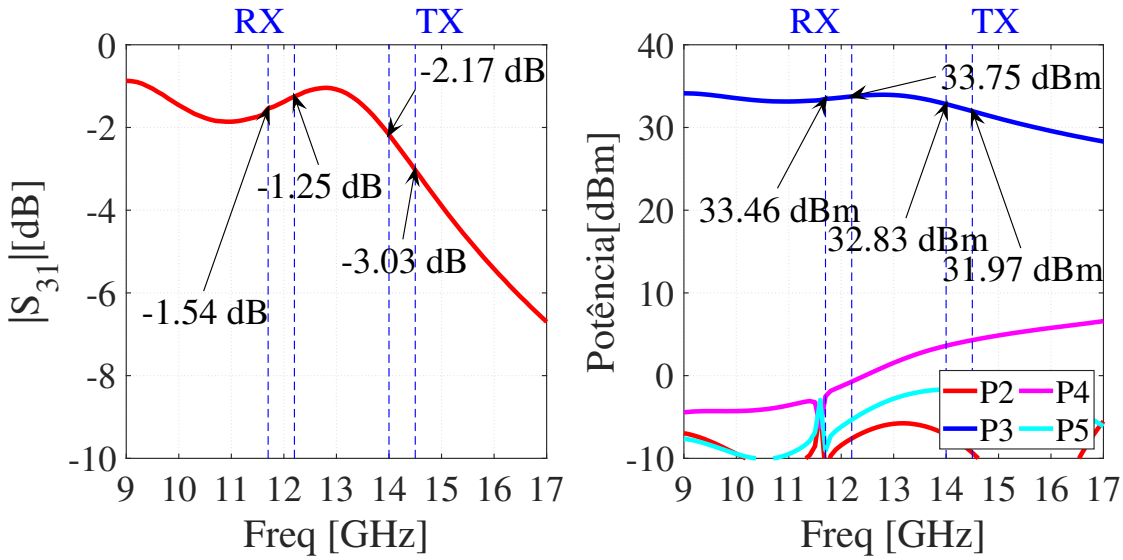


Figure C.7 – LSSP simulation (dB magnitude) for SP4T v1.0 circuit. S_31 on the left, and the power distribution across all ports on the right. Port 1 is the source of the RF signal with a power of 35dBm, and port 3 is connected for the passage of the RF signal. Source: Own elaboration.

Despite not-so-good results, the SP4T v1.0 circuit was manufactured by taking advantage of board space that would not be used. With its assembly, it was found that the tracks that give access to the control pin were very thin, and with the soldering of the *headers* and the heat, these tracks ended up breaking. Although not tested, a test registry was created to verify and compare the simulations.

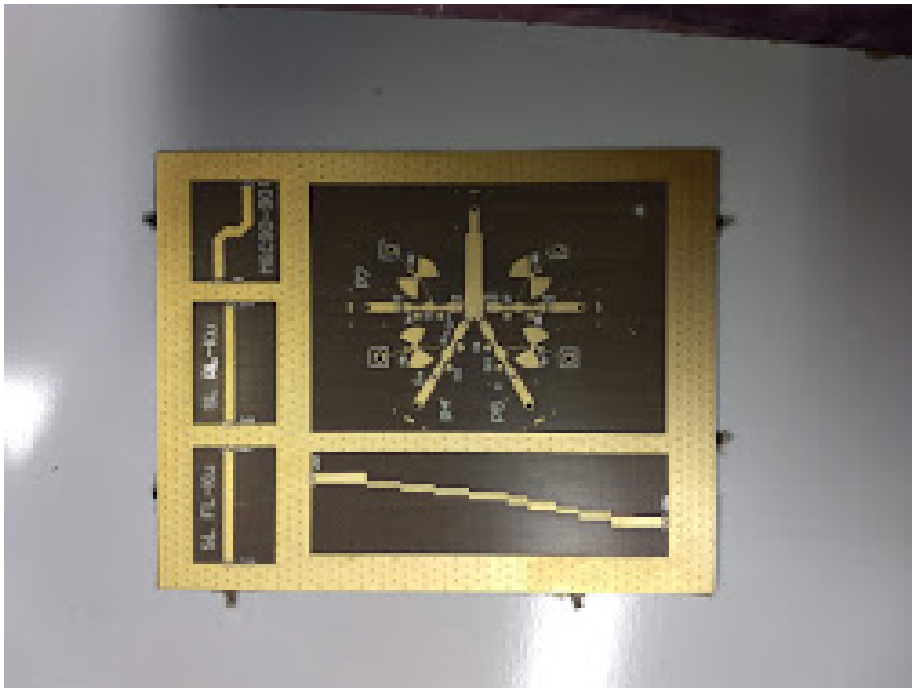


Figure C.8 – Photo of the SP4T v1.0 circuit with tracks connecting the two ground planes. Source: Own elaboration.

C.2 SP4T VERSION 3.0

These are the simulations and *layout* of the third version of the one to four-port switch developed during the project. This version was not satisfactory, as ports 2 and 5 have very different insertion losses than those simulated in ports 3 and 4.

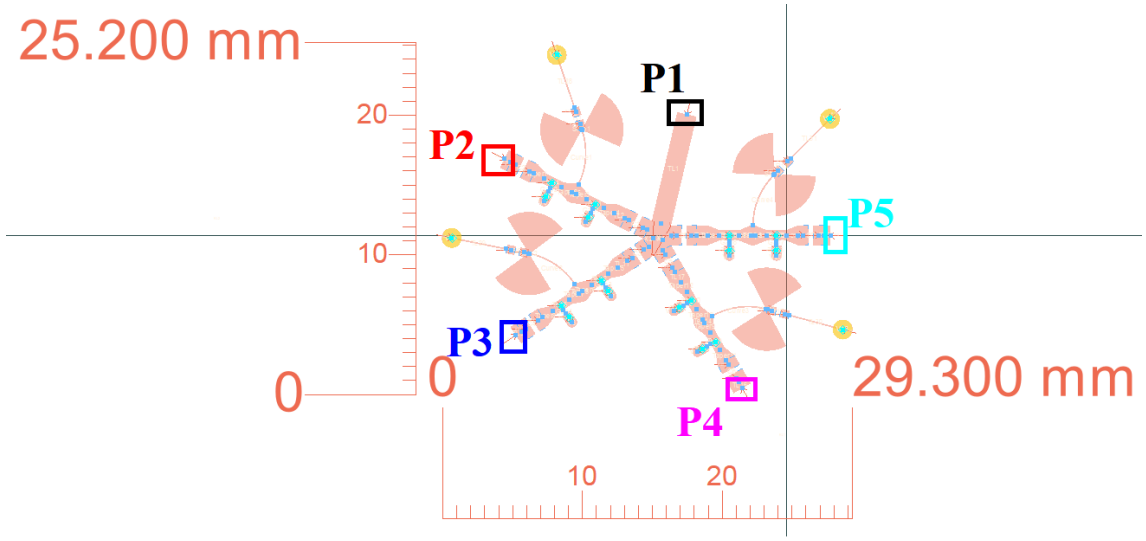


Figure C.9 – SP4T circuit in its third version, showing ports P1 to P5. Source: Own elaboration.

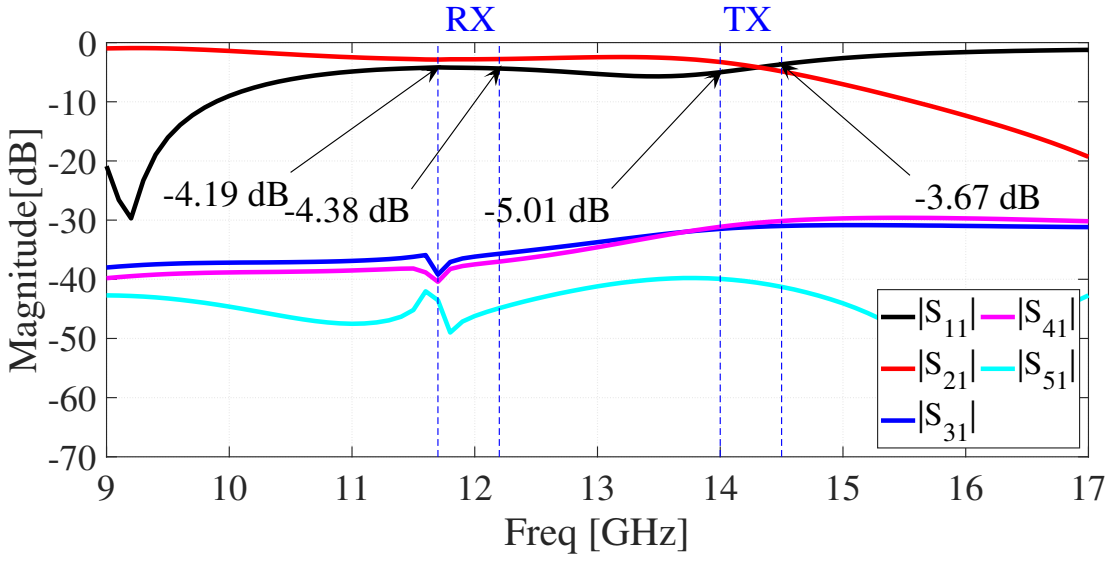


Figure C.10 – LSSP (magnitude in dB) simulation for SP4T v3.0 circuit with projected bias. Port 1 is the source of the RF signal, and port 2 is connected for the passage of the RF signal. Source: Own elaboration.

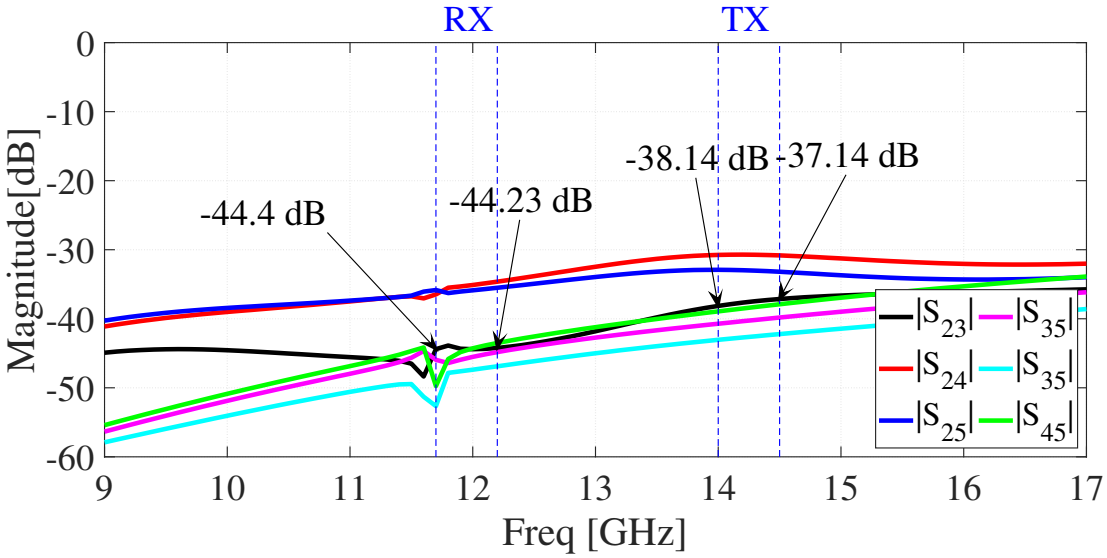


Figure C.11 – LSSP (dB magnitude) simulation for SP4T v3.0 circuit showing isolation between channels. Port 1 is the source of the RF signal, and port 2 is connected for the passage of the RF signal. Source: Own elaboration.

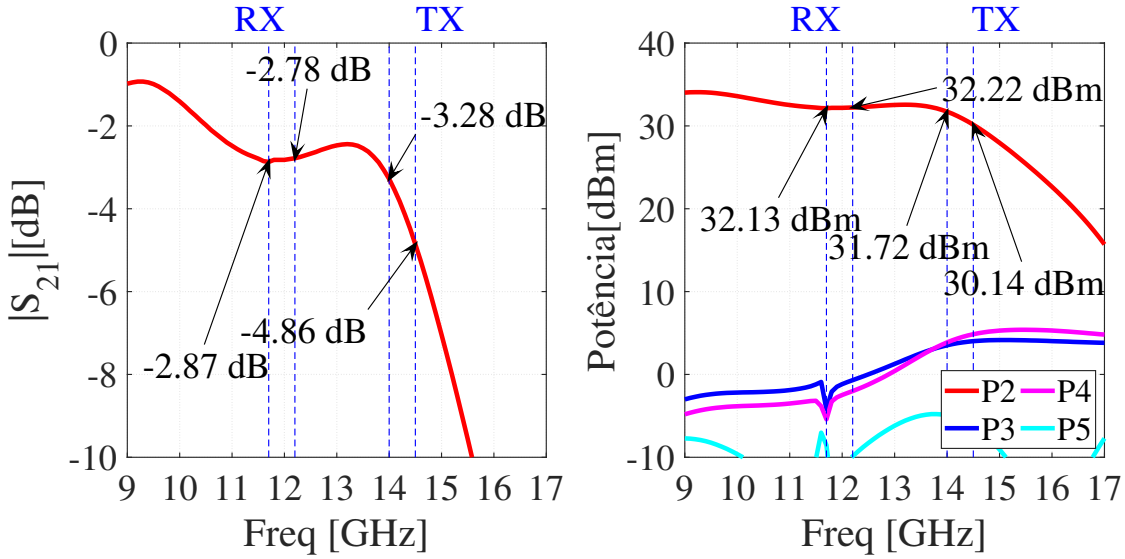


Figure C.12 – LSSP simulation (dB magnitude) for SP4T v3.0 circuit. S_21 on the left, and the power distribution across all ports on the right. Port 1 is the source of the RF signal with a power of 35dBm, and port 2 is connected for the passage of the RF signal. Source: Own elaboration.

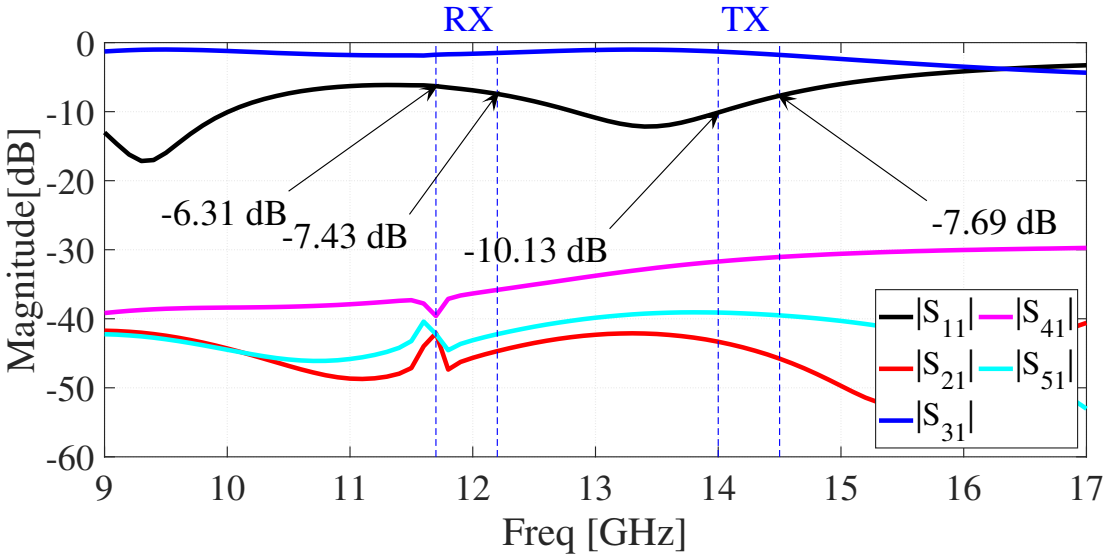


Figure C.13 – LSSP (magnitude in dB) simulation for SP4T v3.0 circuit with projected bias. Port 1 is the source of the RF signal, and port 3 is connected for the passage of the RF signal. Source: Own elaboration.

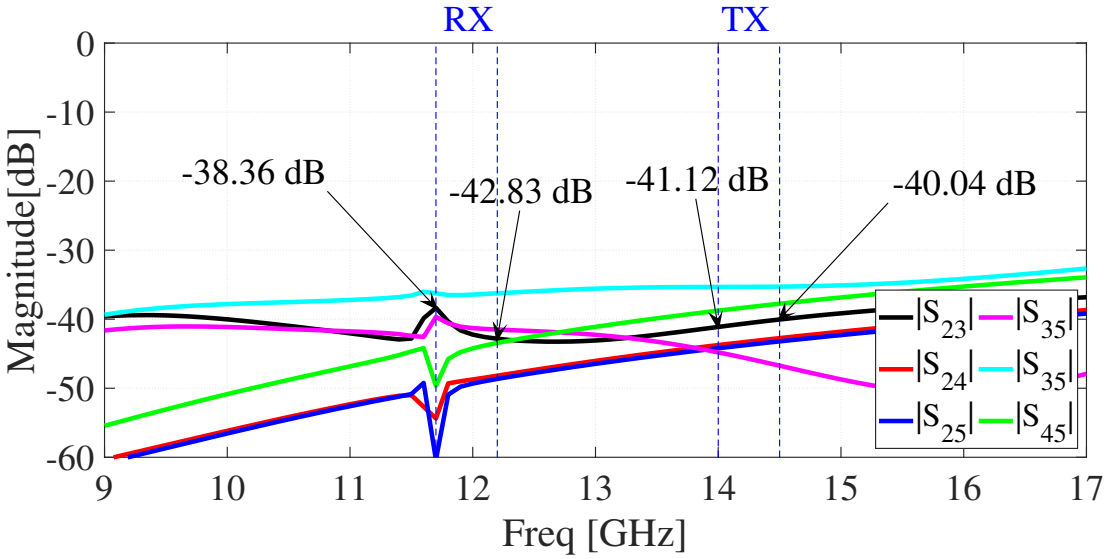


Figure C.14 – LSSP (dB magnitude) simulation for SP4T v3.0 circuit showing isolation between channels. Port 1 is the source of the RF signal, and port 3 is connected for the passage of the RF signal. Source: Own elaboration.

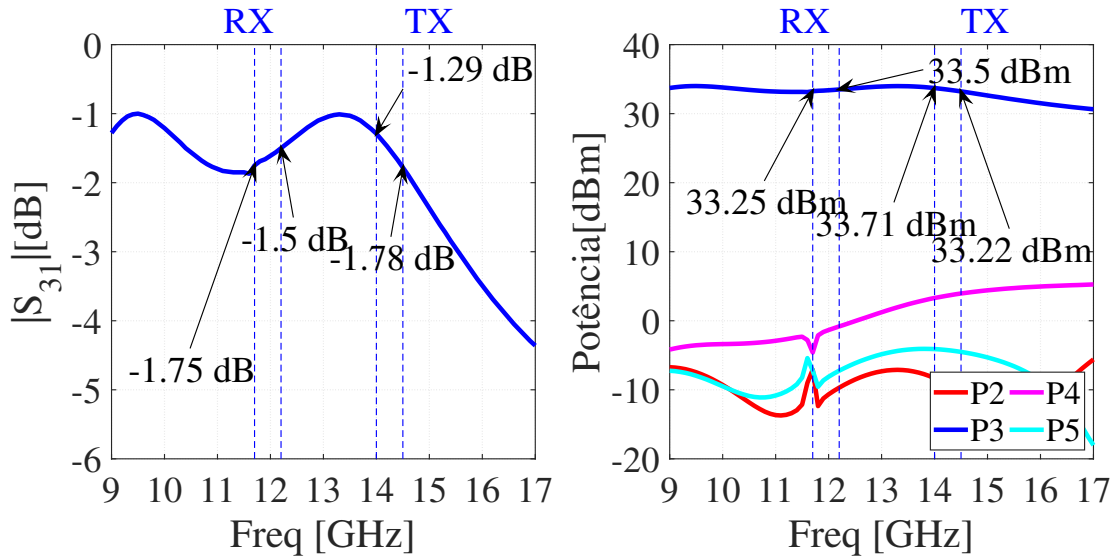


Figure C.15 – LSSP simulation (dB magnitude) for SP4T v3.0 circuit. S_31 on the left, and the power distribution across all ports on the right. Port 1 is the source of the RF signal with a power of 35dBm, and port 3 is connected for the passage of the RF signal. Source: Own elaboration.

C.3 SP4T VERSION 4.0

In this circuit, port 1 is on the lower layer (in green) and is connected to the upper layer (in orange) by a path that cuts the ground plane (in yellow) between the two. This can be seen in Figures C.16 and C.18. As the port channels are the same, the S-parameter simulations are very similar. So the results shown are only for port 5 turned on but adequately represented when the other ports are turned on.

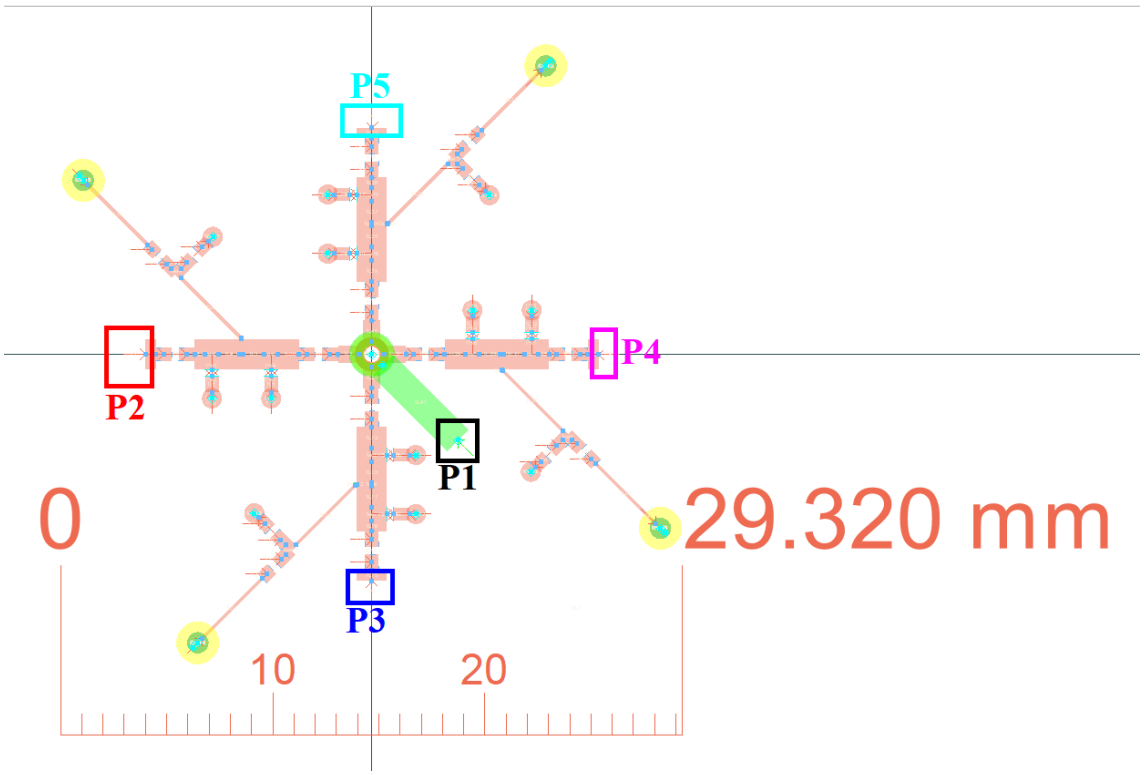


Figure C.16 – SP4T circuit in its fourth version, representing ports P1 to P5. Shown in the figure are port 1 in the lower signal layer in green, the remaining ports in the upper layer in brown, and the ground plane slots in yellow. Source: Own elaboration.

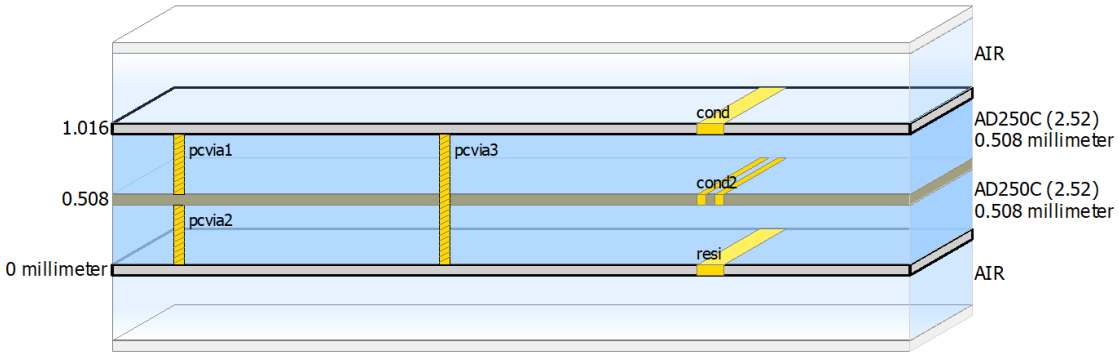


Figure C.17 – Stacking style of 0.508mm AD250C™substrate layers and copper for SP4T v4.0 circuit. The signal layers are the top and bottom conductor layers, and the conductor layer between them is the ground. Source: Own elaboration.

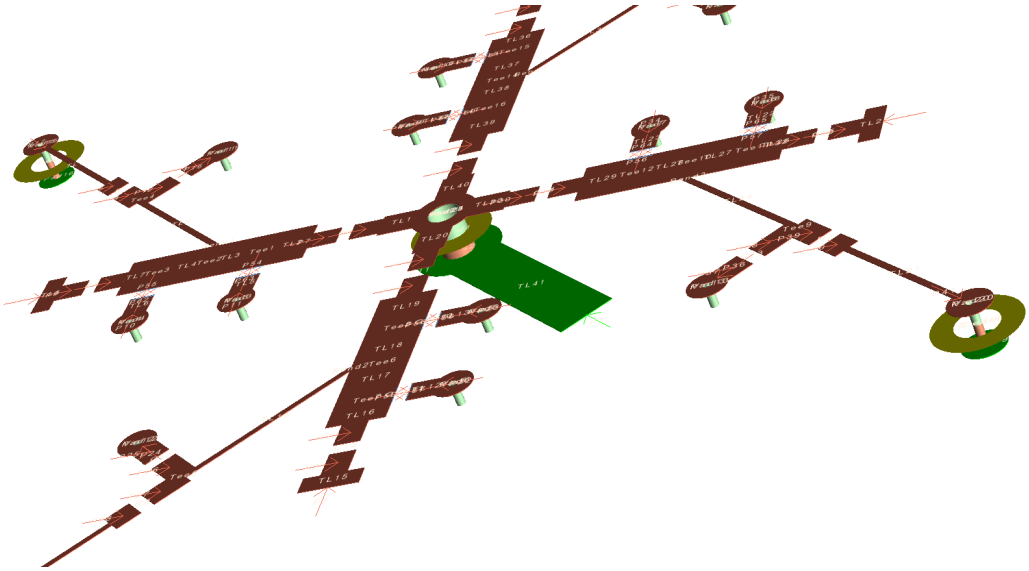


Figure C.18 – Figure of the SP4T v4.0 circuit in perspective in the ADS *Layout* environment. Shown in the figure are port 1 in the lower signal layer in green, the other ports in the upper layer in brown, and the path connecting the two layers. Source: Own elaboration.

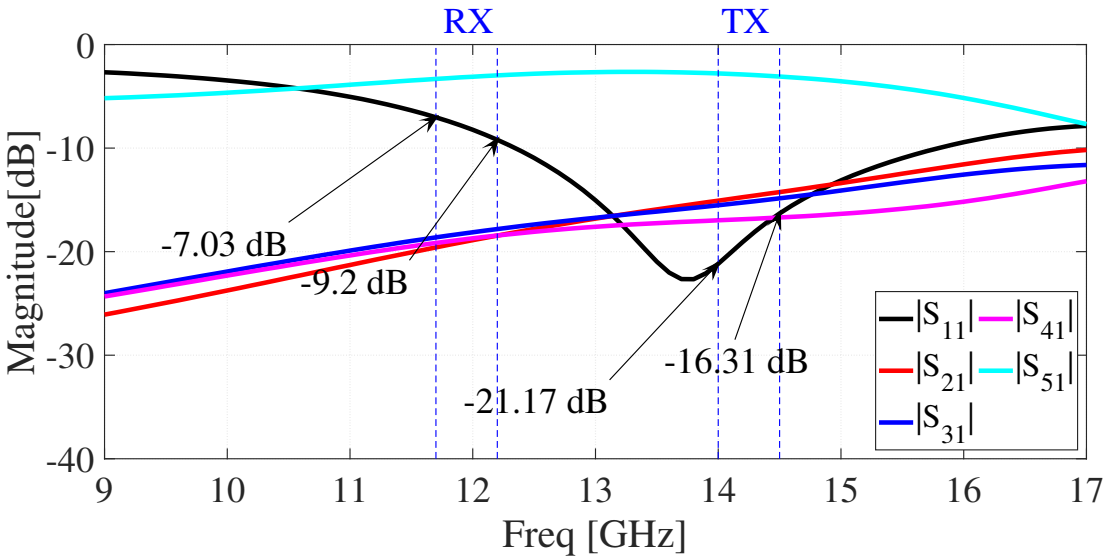


Figure C.19 – LSSP (dB magnitude) simulation for SP4T v4.0 circuit with projected bias. Port 1 is the source of the RF signal, and port 5 is connected for the passage of the RF signal. Source: Own elaboration.

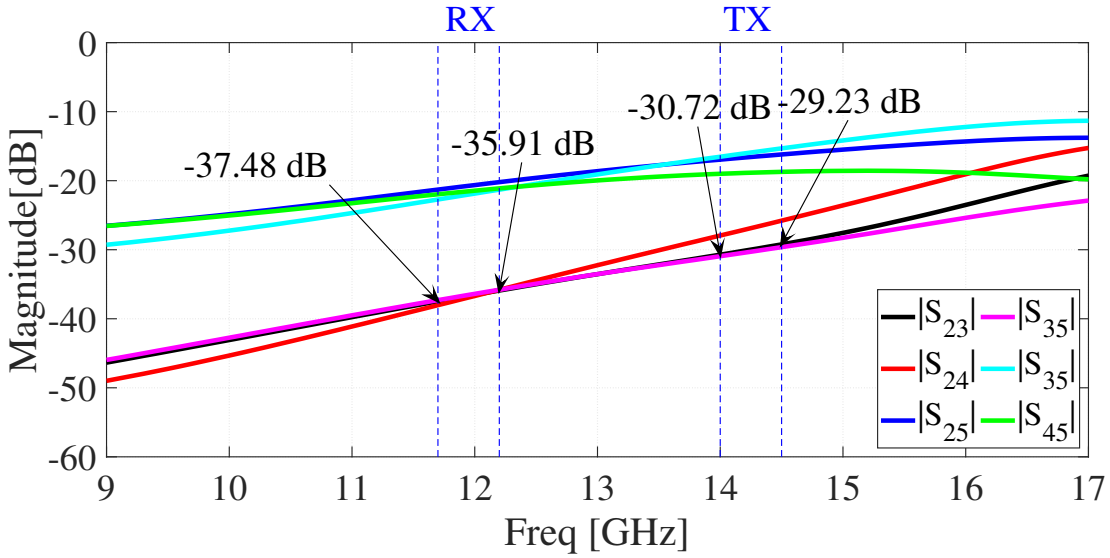


Figure C.20 – LSSP (dB magnitude) simulation for SP4T v4.0 circuit showing isolation between channels. Port 1 is the source of the RF signal, and port 5 is connected for the passage of the RF signal. Source: Own elaboration.

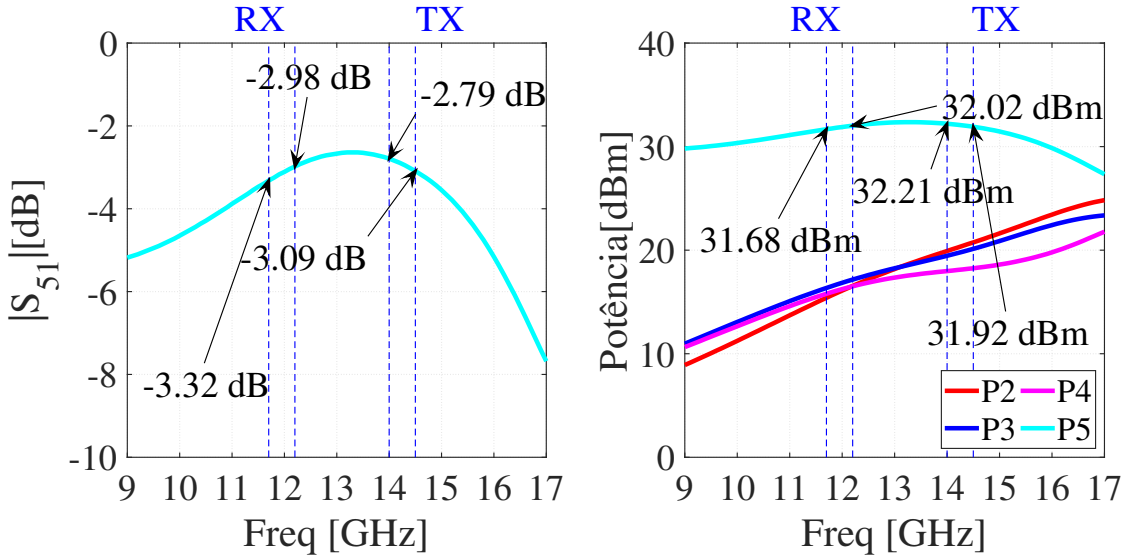


Figure C.21 – LSSP simulation (dB magnitude) for SP4T v4.0 circuit. S_{51} on the left, and the power distribution on all ports on the right. Port 1 is the source of the RF signal with a power of 35dBm, and port 5 is connected for the passage of the RF signal. Source: Own elaboration.

D RF BOARD WITH SPDT SWITCH CIRCUIT

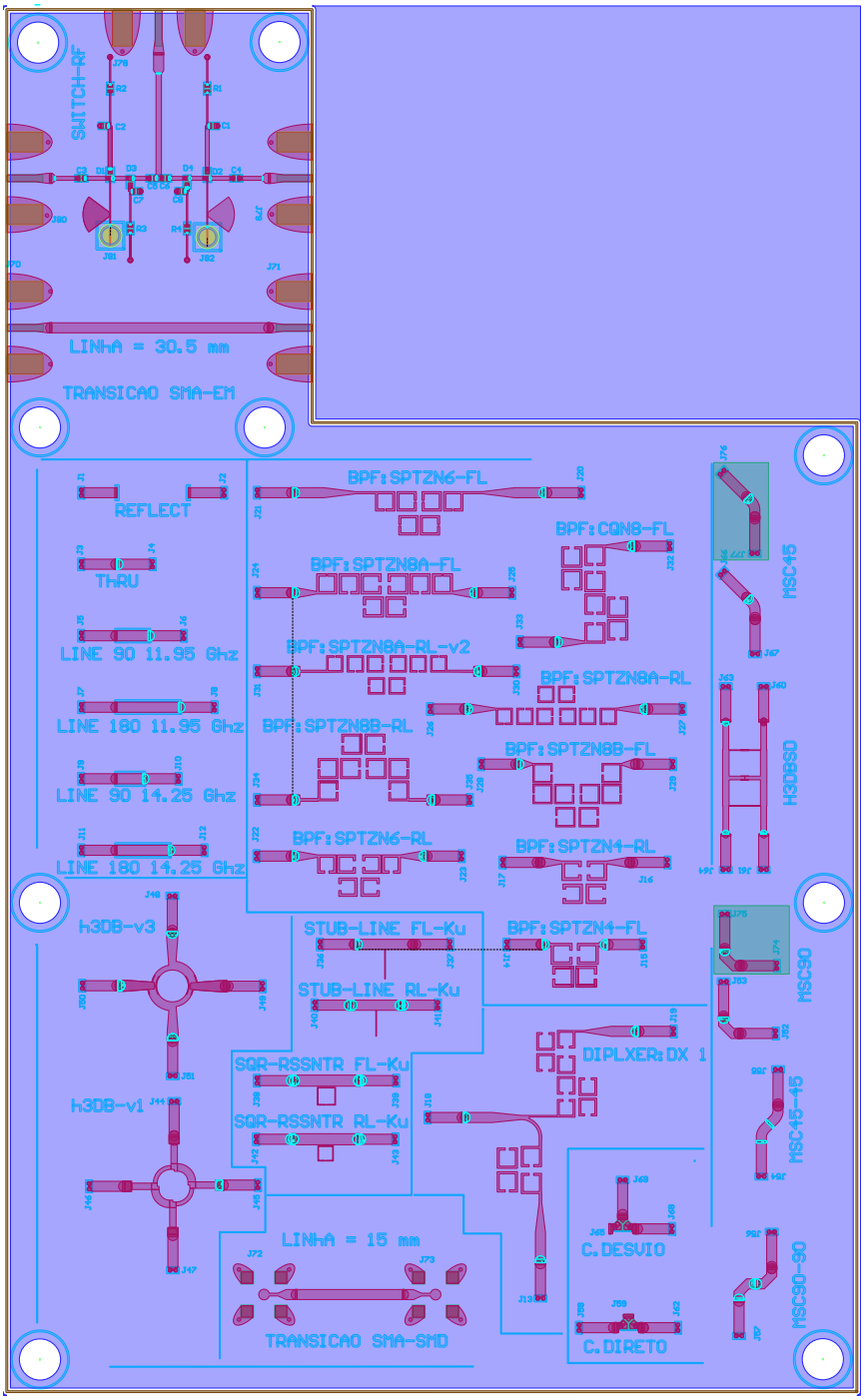


Figure D.1 – RF systems and components board designed with SPDT. Source: Guilherme Felix de Andrade, Matheus Pereira Santana, Vitor Carvalho de Almeida and Vinícius Lisboa do Nascimento.

E RF BOARD WITH SP4T V2.0 SWITCH CIRCUIT

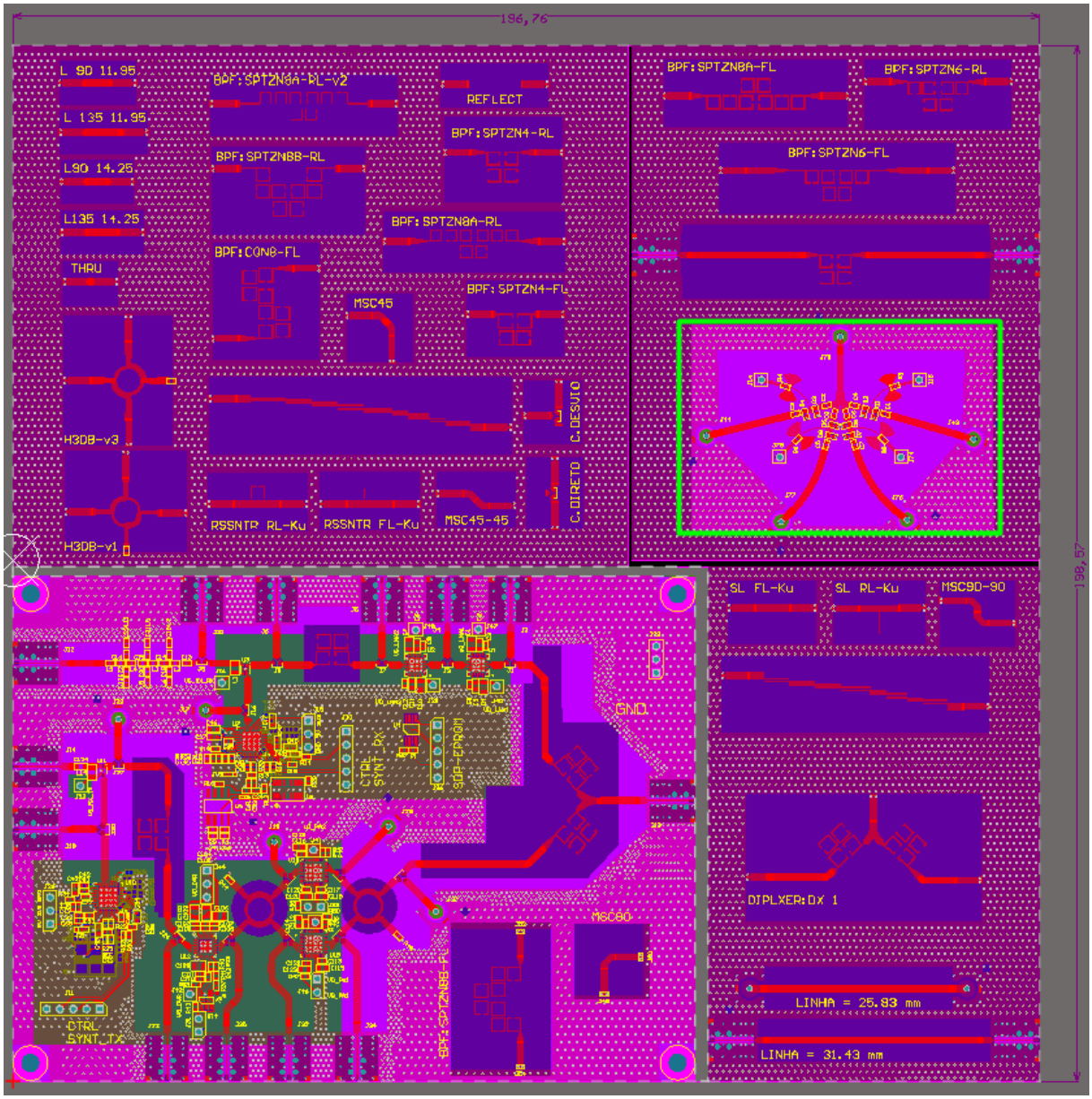
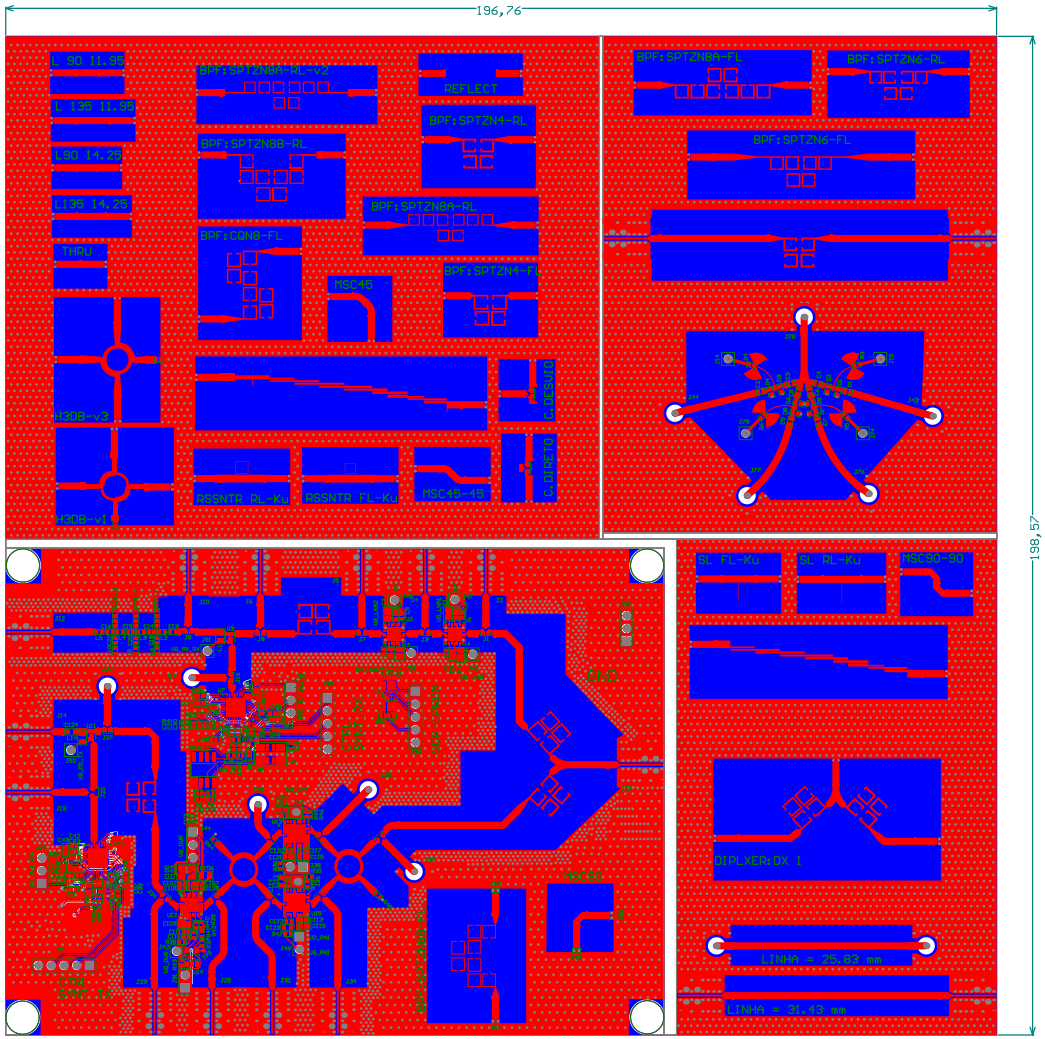


Figure E.1 – RF systems and components board designed with SP4T v2.0. Source: Guilherme Felix de Andrade, Matheus Pereira Santana, Vitor Carvalho de Almeida and Vinícius Lisboa do Nascimento.

PCB SPECIFICATIONS	
MATERIAL:	ROGERS AD250C : 0,508 mm +/- 10%
LAYERS:	Multilayer PCB: 2 layers
PCB Finishing: ☐ HASL (Hot Air Solder Leveling) – IPC-A-600; ☒ ENIG (Electroless nickel immersion gold): 3.0"±0 um (Ni) + 0.05 &Rt; um (Au) – IPC-4552.	
SOLDER MASK:	BLUE
SILKSCREEN: ☒ Top Overlay ☒ Bottom Overlay	
COLOR:	WHITE
VIA FINISHING: ☒ Tenting ☐ Button ☐ Plugged	

NOTES (UNLESS OTHERWISE SPECIFIED):
1 – Dimensions in millimeters. Tolerance +/- 10% and 20um to structure beyond 250um. Spacing tolerance +/- 10% and 30um for spacing beyond 300um
2 – Maximum bending and torsion: 1%;
3 – PCB Electrical Testing not needed;
4 – Use the files sent with the documentation for the drilling process;
5 – Follow MANDATORILY the stack-up and the copper's (Cu) thickness indicated in the LAYER STACK TABLE;
6 – Follow the standard IPC-6012C;
7– For any changing related adding fiducials or reference markings on copper layers, the responsible must be informed before start the production process.



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,010mm	3,5	
3	Top Layer	Copper	0,018mm		
4	Dielectric 1	AD250C	0,508mm	2,5	
5	Bottom Layer	Copper	0,018mm		
6	Bottom Solder	Solder Resist	0,010mm	3,5	
7	Bottom Overlay				

COOPERs	Top Layer		Bottom Layer	
SPECs	Outline	Cotas		Fab(Info
SILKSCREENs	Top Overlay	Bottom Overlay		
STENCILs				
SOLDER MASKs				
OTHERs		Keep-Out Layer		

Projetos:	Antena Communication Unit UNB	Layouts:	Grupo 3
Conteudos:	Pshel – RFBoard– PACBoard	Revisors:	
Datas:	04/06/2019		
		Versaos:	1.1.0
			2

F RF BOARD WITH SP16T SWITCH MATRIX CIRCUIT

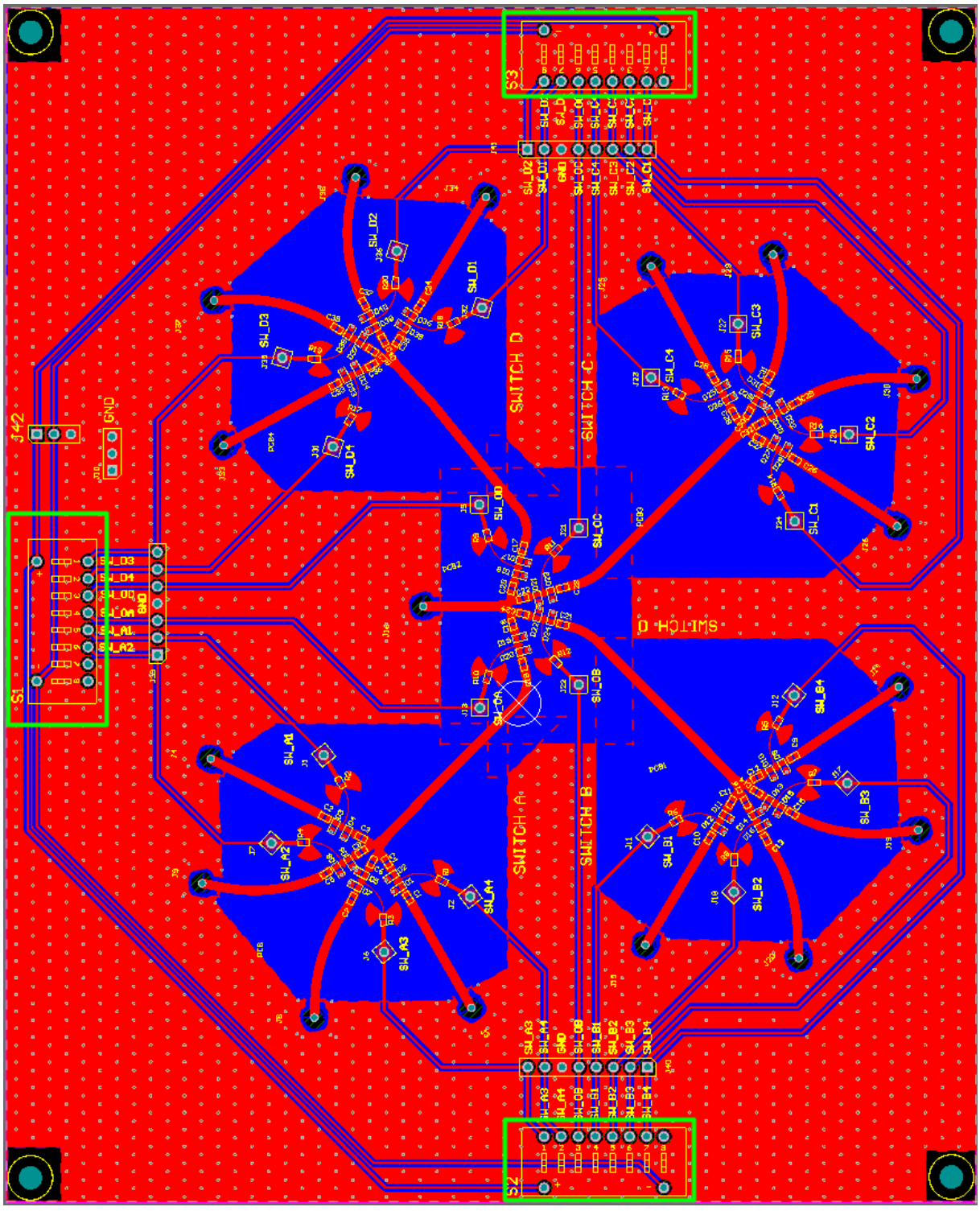


Figure F.1 – RF systems and components board designed with SP16T. Source: Guilherme Felix de Andrade, Matheus Pereira Santana, Vitor Carvalho de Almeida and Vinícius Lisboa do Nascimento.

PCB SPECIFICATIONS

MATERIAL: ROGERS AD250C : 0.508 mm +/- 10%

LAYERS: Multilayer PCB: 2 layers

PCB Finishing:

☐ HASL (Hot Air Solder Leveling) – IPC-A-600J;

☒ ENIG (Electroless nickel immersion gold)

3.0"±0 um (Ni) + 0.05 MIN um (Au) – IPC-4552.

SOLDER MASK: BLUE

SILKSCREEN:

☒ Top Overlay ☐ Bottom Overlay

COLOR: WHITE

VIA FINISHING:

☒ Tenting ☐ Button ☐ Plugged

NOTES (UNLESS OTHERWISE SPECIFIED)

1 – Dimensions in millimeters. Tolerance +/- 10% and 25um to structure beyond 250um.
Spacing tolerance +/- 10% and 50um For spacing beyond 500um

2 – Maximum bending and torsion: 1%;

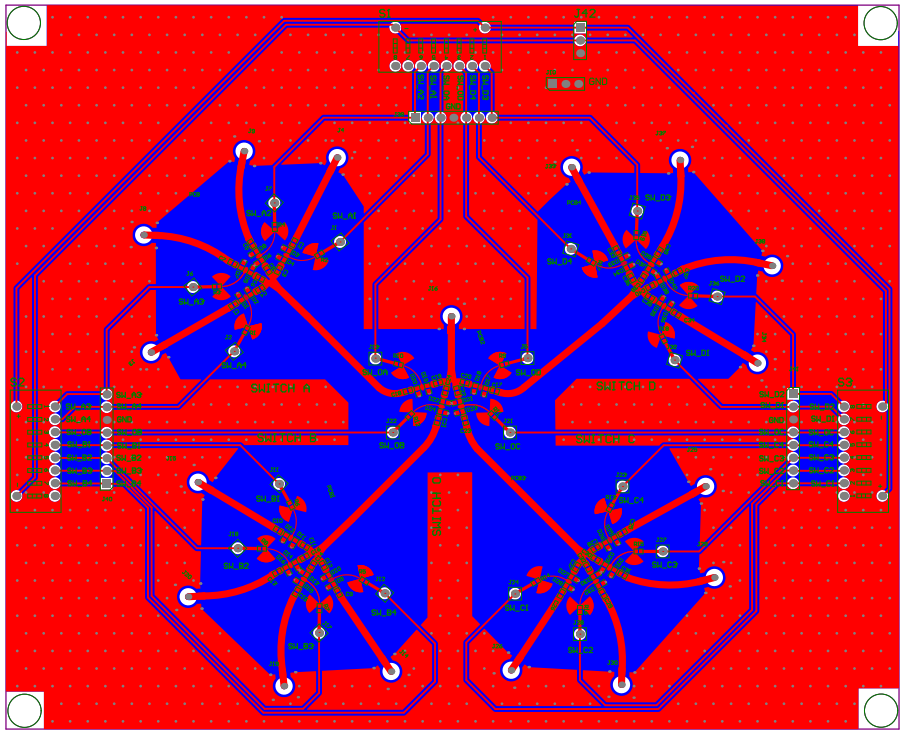
3 – PCB Electrical Testing not needed;

4 – Use the files sent with the documentation for the drilling process

5 – Follow MANDATORILY the stack-up and the copper's (Cu) thickness indicated in the LAYER STACK TABLE;

6 – Follow the standard IPC-6012C

7– For any changing related adding fiducials or reference markings on copper layers, the responsible must be informed before start the production process.



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,40mil	3,5	
3	Top Layer	Copper	0,71mil		
4	Dielectric 1	AD250C	20,00mil	2,5	
5	Bottom Layer	Copper	0,71mil		
6	Bottom Solder	Solder Resist	0,40mil	3,5	
7	Bottom Overlay				

COOPERs	Top Layer		Bottom Layer	
SPECs	Outline			Fabinfo
SILKSCREENs	Top Overlay	Bottom Overlay		
STENCILs				
SOLDER MASKs				
OTHERs		Keep-Out Layer		

Projetos: Projeto		Layouts: Grupo 3	Versaos: 1.1.0
Conteudos: Matriz de Chaveadores		Revisors:	
Datas: 04/06/2019			2