



PhD THESIS

**Design, Optimization and Integration of Doherty Power Amplifier
for 3G/4G Mobile Communications**

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Electrical Engineering Department

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UNIVERSITY OF BRASÍLIA
FACULTY OF TECHNOLOGY

**UNIVERSITY OF BRASÍLIA
FACULTY OF TECHNOLOGY
ELECTRICAL ENGINEERING DEPARTMENT**

**DESIGN, OPTIMIZATION AND INTEGRATION OF
DOHERTY POWER AMPLIFIER FOR 3G/4G MOBILE
COMMUNICATIONS**

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MARCOS LAJOVIC CARNEIRO

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RESUMO

PROJETO, OTIMIZAÇÃO E INTEGRAÇÃO DE AMPLIFICADORES DE POTÊNCIA DOHERTY PARA COMUNICAÇÕES 3G/4G

Os sinais dos novos padrões de comunicação (LTE/LTE-Advanced) apresentam uma elevada diferença entre o pico e a média de sua potência (PAPR), sendo inadequados para o uso com os amplificadores de potência convencionais por apresentarem eficiência máxima apenas quando trabalham com sua potência máxima. Os novos sinais, na maior parte do tempo, demandam médias e baixas potências, concentrando a operação dos amplificadores de potência em uma região de baixa eficiência, o que provoca excessiva dissipação de energia em forma de calor e redução do tempo da bateria.

Os amplificadores de potência Doherty por apresentarem uma eficiência constante por uma larga faixa de potências representam uma solução favorável para o problema da PAPR. Devido à tendência atual de redução dos dispositivos e integração completa da cadeia de RF em um único *chip*, decidiu-se implementar esse amplificador de potência na tecnologia CMOS 65nm por ela já ser adequada à implementação de circuitos digitais, o que permite a integração de um sistema completo.

Este trabalho apresenta a metodologia de projeto e medições de um amplificador de potência Doherty totalmente integrado em tecnologia CMOS 65nm com desempenho de eficiência de potência adicionada (PAE) constante ao longo de uma retração de potência de 7dB. Medidas feitas de 2.4GHz à 2.6GHz mostram o desempenho constante de PAE começando no nível de 20% até 24%, com uma potência máxima de 23,4dBm. O circuito é totalmente descrito com todos os valores de componentes e detalhes de leiaute para posterior reprodução. As curvas que mostram o efeito de modulação ativa de carga, as correntes dos sub-amplificadores e o comportamento constante de PAE demonstram a implementação de um autêntico amplificador de potência Doherty. O circuito foi projetado com atenção especial para o baixo custo, utiliza apenas componentes discretos, cada sub-amplificador possui topologia cascode de saída simples e suas redes de entrada/saída são otimizadas para economizar área de *chip* e produzir um desempenho constante de PAE.

ABSTRACT

DESIGN, OPTIMIZATION AND INTEGRATION OF DOHERTY POWER AMPLIFIERS FOR 3G/4G COMMUNICATIONS

The signals of the new communication standards (LTE / LTE-Advanced) show a great difference between the peak and its average power (PAPR) being unsuitable for use with conventional power amplifiers because they present maximum efficiency only when working with maximum power. These signals demands low and medium power for most part of the time, which concentrates the operation of power amplifiers in a region of low efficiency, resulting in excessive heat dissipation and reduction of battery time.

Doherty power amplifiers for presenting a constant efficiency for a wide power range represent a favorable solution to this problem. Given the current trend of reducing devices and full integration of RF chain on a single chip, it was decided to implement this power amplifier in 65nm CMOS technology due to its performance for digital circuits, allowing the integration of a whole system.

This work presents the design methodology and measurements results of a fully integrated Doherty Power Amplifier in 65 nm CMOS technology with constant PAE over a 7 dB backoff. Measurements from 2.4 GHz to 2.6 GHz show constant PAE performance starting in 20% level up to 24% with a maximum output power of 23.4 dBm. The circuit is fully described with all components values and layout details for further reproduction. Curves showing the active load-pull effect, sub-amplifiers behavior and constant PAE prove that it is a genuine Doherty Power Amplifier. The circuit was designed with special attention to low cost, it is composed by only lumped components, each sub-amplifier has single-ended cascode topology and their input/output networks are optimized to save die area and to produce a constant PAE.

RESUMÉ

CONCEPTION, OPTIMISATION ET INTÉGRATION D'AMPLIFICATEURS DE PUISSANCE DOHERTY POUR DES COMMUNICATIONS 3G/4G

L'amplificateur de puissance (PA) est l'élément qui consomme le plus d'énergie dans les architectures d'émission-réception RF des terminaux mobiles. Les PAs conventionnels ont un rendement maximum seulement au niveau de puissance maximum, tandis que pour des niveaux de puissance plus bas, le rendement des PAs est très faible. Or les nouveaux standards de communications à haut débit (4G/LTE advanced) utilisent des modulations à enveloppe non-constante. Ainsi, le rapport entre la puissance maximum et la puissance moyenne du signal (PAPR – Peak to Average Power Ratio) est élevé. C'est le cas également pour l'OFDM qui possède un fort PAPR avec les porteuses multiples. Ainsi, lorsqu'un signal a un fort PAPR, cela signifie que le rendement moyen du PA utilisé est faible. La conséquence directe est la rapide décharge des batteries des terminaux mobiles.

L'Amplificateur de Puissance Doherty (APD) est une technique connue d'amélioration du rendement. Cette technique permet d'augmenter le rendement moyen des amplificateurs en améliorant le rendement aux faibles niveaux de puissance, tout en maintenant le rendement maximum sur une plus grande plage de puissance de sortie. Cette technique est bien adaptée pour résoudre le problème de rendement pour les signaux à forts PAPR. De nombreux travaux proposent des solutions intégrées des APD dans une technologie à faible coût, mais au détriment du maintien d'un rendement à puissance ajoutée (Power Added-Efficiency, PAE) constant sur une grande plage de puissance.

Nos travaux de recherche proposent un APD totalement intégré en technologie 65nm CMOS de STMicroelectronics à 2,535 GHz avec une PAE constante sur une plage de recul en puissance de sortie de 8 dB. Pour la conception de cet amplificateur, nous avons utilisé sept niveaux de métaux sur les dix couches de métaux de la technologie, les capacités sont de type MOM afin de respecter des contraintes faible coût.

Le principe de l'APD est d'utiliser l'effet connu sous le nom de « load-pull actif » : une charge vue par une source de courant peut être modifiée par l'application d'un courant provenant d'une deuxième source. Pour atteindre cet objectif, l'architecture Doherty utilise

deux amplificateurs de classes différentes en parallèle. Le PA principal (classiquement polarisé en classe B ou AB) fonctionne pour tous les niveaux de puissance et le PA auxiliaire (classiquement en classe C) ne fonctionne que pour les niveaux de puissance moyens et forts. L'augmentation de rendement s'explique par la transformation d'impédance de drain du PA principal, à cause de la combinaison de deux facteurs en même temps, la charge inversée vue par la ligne de transmission d'un quart d'onde et le courant du PA auxiliaire qui augmente. En effet, lorsque le courant du PA auxiliaire augmente, l'impédance vue par le PA principal se réduit.

L'APD a été conçu avec les transistors à drain étendu haute tension pour soutenir une grande excursion de tension et produire des niveaux de puissance de sortie plus élevés. Les limites de V_{dd} et V_{gs} du transistor sont de 2.75V et de 5.5V, respectivement. Chaque sous-amplificateur a été conçu avec une topologie cascode pour donner au PA une meilleure isolation vis-à-vis des effets de désadaptation d'impédances entre la sortie et l'entrée. De plus, cette topologie permet d'avoir une plus grande tension d'alimentation V_{dd} par rapport à la topologie source commune.

Les deux amplificateurs, principal et auxiliaire, ne sont cependant pas identiques. En effet, les dimensions des transistors dépendent du courant traversant chaque amplificateur. Ainsi, le transistor grille commune du PA principal est constitué de 28 transistors en parallèle, tandis que le transistor source commune du PA principal est composé de 26 transistors en parallèle. Pour le PA auxiliaire, le transistor grille commune est composé de 26 transistors en parallèle et son transistor source commune est composé de 14 transistors en parallèle.

Chaque sous-amplificateur a été conçu et optimisé individuellement en prenant en compte les réseaux d'adaptation, l'inductance d'arrêt, les impédances d'entrée prévues par le diviseur de puissance et l'impédance de sortie prévue pour avoir l'effet loadpull actif de l'APD. Tout au long du travail de conception, les performances des deux PAs ont été tracées sur le même graphique pour équilibrer correctement le point de compression de chacun. Les courbes de PAE de chacun ont été optimisées dans le but de produire un APD avec une PAE constante sur une large gamme de puissance.

Après la connexion des sous-amplificateurs dans le même schéma électrique, les lignes de transmission à éléments localisés ont été ajoutées, puis la topologie a été ré-optimisée pour

réduire le nombre d'inductances et ainsi réduire l'espace utilisé dans la puce. À l'entrée, le diviseur de Wilkinson, la ligne de transmission déphasage et les réseaux d'adaptation d'entrée des PAs principal et auxiliaire ont été fusionnés et optimisés. À la sortie de l'APD, les réseaux d'adaptation de sortie des deux PAs et la ligne de transmission d'inversion de charge ont aussi été fusionnés et optimisés. Pour atteindre l'objectif d'avoir une PAE constante, une méthodologie d'optimisation séquentielle a été appliquée pour bien équilibrer tous les éléments dans le schéma de l'APD en respectant toutes les limites de tensions des transistors. Le circuit a été implémenté dans une surface de $1,72 \times 1,68 \text{ mm}^2$. Il a été conçu pour être mesuré avec des sondes directement positionnées sur les trois différents types de plots.

Ce travail présente la méthodologie de conception et des résultats de mesure d'un amplificateur de puissance Doherty entièrement intégré dans la technologie 65 nm CMOS avec une PAE constante sur 7 dB de plage de puissance. Les mesures de 2,4 GHz à 2,6 GHz montrent des performances constantes en PAE de 20% jusqu'à 24% avec une puissance de sortie maximale de 23,4 dBm. Le circuit est entièrement décrit avec les valeurs des composants et les détails de layout pour permettre sa reproduction. Ce travail montre l'effet de modulation active de charge, le comportement en courant des sous-amplificateurs et la performance constante en PAE, ce qui démontre l'implémentation d'un véritable amplificateur de puissance Doherty. Le circuit est composé uniquement d'éléments localisés, et les réseaux d'entrée et de sortie sont optimisés pour réduire la taille de la puce et pour produire une PAE constante.

L'amplificateur de puissance Doherty présenté est le premier APD totalement intégré en technologie 65 nm CMOS avec une PAE constante sur une large gamme de puissance. Il respecte de ce point de vue la théorie de Doherty. La comparaison avec un amplificateur de puissance classique polarisé en classe AB montre une amélioration de la PAE pour les niveaux de faible et moyenne puissance, permettant ainsi d'augmenter nettement le rendement moyen de l'amplificateur. Aucun autre APD publié ne présentait ce type de caractéristique en rendement dans cette technologie. La technologie 65nm CMOS est généralement plus appropriée pour les applications numériques, par conséquent, l'utilisation de cette technologie s'inscrit dans la tendance actuelle du développement d'un système complet sur une seule puce, où les étages numérique et analogique sont intégrés sur la même puce silicium.

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LIST OF SYMBOLS, NOMENCLATURES AND ABBREVIATIONS

3G/4G	-	Third/Fourth generation
3GPP	-	3rd Generation Partnership Project
ACLR	-	Adjacent channel leakage ratio
ACPR	-	Adjacent-Channel Power Ratio
ADS	-	Advanced Design System
BTS	-	Base station
CDMA	-	Code Division Multiple Access
CG	-	Common Gate
CP	-	Cyclic prefix
CS	-	Common Source
DFT	-	Discrete Fourier Transform
DK	-	Design Kit
DPA	-	Doherty Power Amplifier
EER	-	Envelope elimination and restoration
ET	-	Envelope Tracking
FDMA	-	Frequency Division Multiple Access
IDFT	-	Inverse Discrete Fourier Transform
IMD	-	Inter modulation distortion
LTE	-	Long Term Evolution
MIMO	-	Multiple input multiple output
OFDM	-	Orthogonal Frequency Division Multiplexing
OFDMA	-	Orthogonal Frequency Division Multiplexing Access
PA	-	Power Amplifier
PAE	-	Power added efficiency
PAPR	-	Peak-to-Average Ratio
PBO	-	Power backoff
PCB	-	Printed circuit board
PLS	-	Post-Layout simulation
RF	-	Radio frequency
SC/FDE	-	Single carrier with frequency domains equalization
SC-FDMA	-	Single Carrier Frequency Division Multiple Access
SoC	-	System on Chip

- TDMA - Time Division Multiple Access
- WiMAX - Worldwide Interoperability for Microwave Access
- WWAN - Wireless Wide Area Network

2 INTRODUCTION

2.1 MOTIVATION

The telecommunication market observes nowadays a growing demand for radio frequency (RF) mobile devices. One of the major requirements of these systems is the high efficiency on energy use in order to extend the battery life in mobile devices. Among the main RF transmission subsystems, power amplifiers (PA) found in transmitters have been recognized as one of the RF chain blocks that dissipates most energy [1].

Conventional PAs class A, B, AB and C present maximum efficiency only at maximum output power level. As long as the signal power decreases, the amplifier efficiency also decreases and very quickly. The new communication standards LTE/LTE-Advanced (4G standard) [2] presents amplitude modulation which makes conventional PAs to work with an average efficiency much less than its maximum.

Another characteristic of these new communication standards is the high peak-to-average power ratio (PAPR). Communication systems evolution have been heading towards the use of several sub-carriers in transmission using orthogonal frequency division multiplexing (OFDM) due to its robustness in channels that presents high variations, frequency selectivity and multipath. The high PAPR characteristic makes the signal to stay in low and medium power levels most of the time, where conventional PAs have a very low efficiency. In theory, an OFDM signal with 52 sub-carriers has a 17dB PAPR [3]. The use of communication standards with high PAPR in a conventional PA makes it to work with a low efficiency level, which decreases the battery life and produce high energy dissipation (heating) [4] [1] [5].

For these reasons, the 4G standard has chosen the single carrier frequency division multiple access (SC-FDMA) at the uplink [6], with maximum output power of 23dBm [7], QPSK and 16-QAM modulation [8], presenting a maximum PAPR of 7.03dB on the 16-QAM [9]. Therefore, all effort towards increasing the efficiency on the transmission of high PAPR signals, increasing PA efficiency at low and medium output power levels is of great interest to the mobile telecommunication industry.

Beyond the demand on increasing the battery time of use, the market has been demanding the increase of functions inserted into these devices and its price reduction. This demand indicates the integration trend of multiple circuits, both digital and analog, inside the same chip (system-on-chip, SoC) and the use of low cost silicon based technologies.

2.2 PROPOSED SOLUTION

In order to design a PA more suitable for high PAPR signals (3G/4G), Table 2.1, and to comply the integration and low cost trend, this work proposes the design of an optimized Doherty Power Amplifier (DPA) with all its components integrated in Complementary Metal-Oxide Semiconductor (CMOS) 65nm technology from STMicroelectronics.

Table 2.1 – PAPR for 3G/4G Standards

Standard	PAPR
3G UMTS - WCDMA [10]	3dB
UMTS 3G extension - HSPA [10]	4.9 - 7.2dB
4G LTE uplink – SC-FDMA [10]	7.03dB

The DPAs represent an efficiency enhancement technique [1] for PAs used to maintain the efficiency (transistor’s drain efficiency and power added-efficiency – PAE) at a constant level inside a range of output power values, starting from the maximum output power level until low/medium levels, to cover all demanded levels by the signal standard (amplitude modulated signal). So, even with a high PAPR, the PA remains inside a same PAE level. Other advantage of the DPA is the fully analog control of the efficiency enhancement on the backoff. Efficiency enhancement with digital control reduces the bandwidth and increases circuit size and complexity. The DPA topology also does not exclude the application possibility of other techniques to increase the efficiency and/or linearity performance.

The 65nm CMOS technology of STMicroelectronics is better suited for digital circuits, due to its reduced thickness (12.9 μ m total thickness for 12 metal layer technology [11]), being therefore, a challenge for PAs implementation. The DPA is a technique widely used for radio-base stations [12] [13] [14], normally implemented in printed circuit boards (PCBs). Many works have already attempted to fully integrate a DPA into low cost technologies [3] [15] [16]

[17], however the DPA essential characteristic of constant PAE has not been implemented with full integration in CMOS 65nm technology, allowing the PA integration with other circuits of the RF transmission chain on the same chip.

This work proposes the fully integration of a low cost DPA in CMOS 65nm technology of STMicroelectronics for mobile applications with high PAPR characteristic (3G/4G). Specifications are defined for the last mobile communication standard, the LTE, (official standard 3GPP TS 36.104 V8.4.0), shown in Table 2.2. The frequency chosen for the design is the 2.535GHz (LTE uplink standard central frequency for Europe, Asia and Brazil) and among the DPA main specifications (Table 2.3) there are the constant PAE performance with more than 8dB output power backoff range and with maximum output power of 23dBm (design simulation). The circuit measures presented a constant PAE inside a 7dB backoff range in a frequency band of 200MHz, starting at 2.4GHz up to 2.6GHz, and 23.5dBm output power.

Table 2.2 – LTE specifications

LTE specifications	
Source (Standard): 3GPP TS 36.104 V8.4.0	
Specification	Value
Frequency	2500MHz – 2570MHz
Modulation (uplink)	QPSK, 16-QAM, 64-QAM
PAPR	7.03dB [7]
Output power (uplink)	23dBm [5]
Band	1.25 – 2.5 – 5 – 10 – 15 or 20MHz

The goal of this work is to develop a fully integrated DPA with a high backoff range according to the Doherty theory [1]. In the state of the art, it has not been showed in this technology [3] [15] [16] [17]. As a secondary objective, efforts were made in order to keep the low cost characteristic. The design of integrated circuits in CMOS technology allows the use of many metal layers in the chip, which can considerably raise the production cost. The 65nm CMOS technology allows using up to ten metal layers and MIM capacitors (high quality factor and small area). In order to avoid costs increase, only seven standard layers and MOM capacitors (fringe capacitors, low quality factor and large area) were used, which corresponds to 7.500 euros/mm² (price in the year 2012), Table 2.4. This price is for the

production of a prototype (25 samples of the chip are produced), for a large production the cost depends on several details and reduces drastically when divided by the number of chips. The DPA circuit was fully integrated: input and output network matching, transmission lines, choke inductances (RF block) and power splitter. The design methodology approach was based in optimization techniques [18] [19] employed on many stages of the design, specially the gradient and hybrid method, from the schematic of each sub-PA that composes the DPA, until its complete schematic, layout and re-optimization with electromagnetic models.

Table 2.3 – Design specifications, objectives and restrictions

Power amplifier topology	Doherty Power Amplifier
Integration degree	Fully integrated
Low cost characteristics	Silicon technology (65nm CMOS)
	Only standard metal levels
	MOM capacitors
	Chip area: 3mm ²
Frequency	2.535GHz (LTE: Europe, Asia, Brazil)
Performance	Constant PAE on the LTE uplink PAPR (7dB)
	Output power: 23dBm

Table 2.4 – CMP prices in 2012 for integrated circuits prototypes designed with standard options [20]

65nm CMOS	7500 Euros/mm ² (*) (if Area less or equal to 5mm ²)
	37500 Euros + [(Area-5) * 6000 Euros] (if 5mm ² < Area < 15mm ²) (**)

*Minimum charge is the price of 1 mm². (X*Y)

**Contact CMP for a price quotation when area is larger.

2.3 STATE-OF-THE-ART

The DPA proposed by William H. Doherty in 1936 [21] which consisted on the use of two amplifiers with valves and a ¼ wave line to produce the effect of active load modulation,

remained forgotten during several years until the research been retrieved by Raab in 1987 [22]. Since then, many works with this topology have been published with different technologies. Table 2.5 presents the state-of-the-art of fully integrated DPAs in CMOS 65nm and 90nm technology with frequencies near to 2.5GHz.

Table 2.5 – Comparing the State-of-The-Art of Fully Integrated Doherty Power Amplifiers in CMOS Technology (measurements results)

Ref.	Freq. [GHz]	Gain [dB]	PAE max [%]	PAE @7dB-PBO[%]	PAE reduction @ 7dB-PBO[%]	Psat [dBm]	Technology [nm]
[15]	3.65	26	35	10	-25	26.5	90
[16]	2.4	17	27	15	-12	20.5	90
[17]	2.4	17	33	22	-11	26.3	90
[3]	2.4	27	34	21	-13	30.5	65

DPAs [15] [16] [17] [3] present considerable reduction in PAE performance between their level at the maximum output power and at a 7dB backoff (PBO). The presented PAE performance shows only a small increase in relation to a conventional class AB/B PA. The measured PAE performance does not present the expected shape of a DPA by the theory [4] [1], which corresponds to a two peak curve with a small valley inside, being almost constant in a range (Figure 2.1). The only published fully integrated DPA in 65nm CMOS technology in a near frequency to this research is [3], but, as the others, it presents the same mischaracterization problem of the required constant PAE.

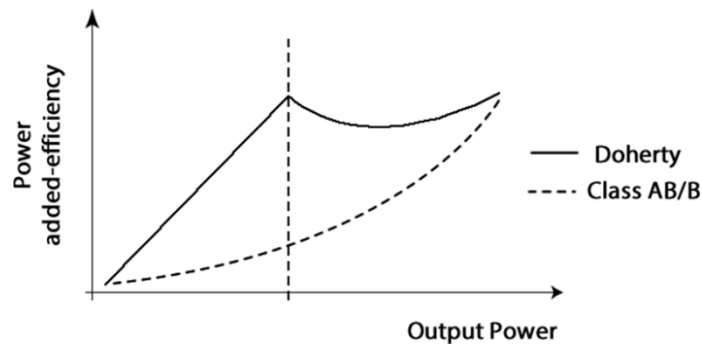


Figure 2.1 – Comparing Doherty and Class AB/B power amplifier PAE performance shape

The DPA implementation needs two PAs connected in parallel by a large network matching to produce the load modulation [1] and the signal dephasing at the input of the auxiliary PA. This last PA needs to be biased on class C which reduces the output power and gain. Due to

these characteristics, it is not attractive to design a DPA without its main goal, which is the constant PAE curve, as has been presented by the state-of-the-art.

This work has the objective to show the feasibility to implement a DPA with closer characteristics to the theoretical DPA with the required performance specifications, fully integration and low cost, for signals with high PAPR due to improve mobile devices to the 3G/4G standard.

2.4 THESIS ORGANIZATION

This thesis starts, in chapter 2, with the evolution of the mobile telecommunications and the LTE standard. The chapter is focused on the probability distribution function of many signals and the characteristics of the OFDM and SC-FDMA. Following, the 65nm CMOS technology is presented with its challenges.

Chapter 3 presents conventional classes of PAs, equations for measurements, topologies and efficiency enhancement techniques. This chapter presents also the DPA design methodology, its equations and a bibliographic revision.

Chapter 4 discusses in a practical way the conventional design and integration methodology for PAs and proposes a new approach for DPAs based on the use of sequential optimizations. All components of the circuit and design stages are presented, the employment of the optimization techniques is explained and layout details are given. Finally, the methodology of re-optimization with electromagnetic models is showed.

The chapter 5 presents the fabricated chip, the measurement setup and the measured performance. Performance comparisons are done between schematic, layout and measures and also between the designed chip and the state-of-art of the fully integrated DPAs in CMOS. Chapter 6 presents final conclusions, reached objectives and proposed challenges for futures works.

2.5 LIST OF PUBLISHED PAPERS OF THIS RESEACH

Carneiro, M. L. ; Deltimple, N. ; Kerhervé, E. ; Carvalho, P. H. P. ; Belot, D. . “A 2,535 GHz Fully Integrated Doherty Power Amplifier in CMOS 65nm with Constant PAE in Backoff”.

4th IEEE Latin American Symposium on Circuits and Systems (LASCAS), DOI: 10.1109/LASCAS.2013.6519031, ISBN: 978-1-4673-4897-3, 27 February - 1 March, Cusco, Peru, 2013.

Carneiro, M. L. ; Deltimple, N. ; Belot, D. ; Carvalho, P. H. P. ; Kerhervé, E. . “Amplificateur de puissance Doherty totalement intégré en CMOS 65nm avec une PAE constante sur une large plage de puissance ». 18ème Journées Nationales Microondes, Paris, France, 2013.

Carneiro, M. L. ; Deltimple, N. ; Belot, D. ; Carvalho, P. H. P. ; Kerhervé, E. .”Fully Integrated Doherty Power Amplifier Electromagnetically Optimized in CMOS 65nm with Constant PAE in Backoff”. 11th IEEE International NEWCAS Conference, DOI: 10.1109/NEWCAS.2013.6573582, ISBN: 978-1-4799-0618-5, 16-19 June, Paris, France, 2013.

Carneiro, M. L. ; Carvalho, P. H. P. ; Deltimple, N. ; Brito, L. C. ; Menezes, L.R.A.X ; Kerhervé, E. ; Araújo, S. G. ; Rocha, A. S. . “Doherty Amplifier Optimization Using Robust Genetic Algorithm and Unscented Transform”. 9th IEEE International NEWCAS Conference, DOI: 10.1109/NEWCAS.2011.5981223, ISBN: 978-1-61284-135-9, 26-29 June, Bordeaux, France, 2011.

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Carneiro, M. L. ; Deltimple, N. ; Belot, D. ; Carvalho, P. H. P. ; Kerhervé, E. ; “Fully Integrated Doherty Power Amplifier in CMOS 65nm with Constant PAE in Backoff”. Analog Integrated Circuits and Signal Processing International Journal, 2014. (under review)

3 FOURTH GENERATION MOBILE COMMUNICATIONS AND CMOS TECHNOLOGY

3.1 INTRODUCTION

When telecommunications signals had no amplitude modulation, the low efficiency of the PAs at the low power region was not a problem; PA operates only in a high efficiency region. With communication standards evolution, the PAPR increased which created the nowadays problem of low efficiency. To contextualize and delimit this research, this chapter presents details of the OFDM signal, which is the communication scheme with higher PAPR, and the SC-FDMA (single carrier frequency division multiple access), which was the chosen standard for the LTE uplink. Following, the 65nm CMOS technology is presented with its main characteristics, advantages and disadvantages.

3.2 MOBILE COMMUNICATIONS EVOLUTION

The last decade showed an accentuated growth in the wireless communication systems industry. As the communication systems evolved, different standards were classified in terms of generation following a chronological order, as shown on Figure 3.1.

The first generation (1G) corresponds to the first analogic mobile communications systems emerged around 1980. These systems were primarily projected to voice transmission, but also had a small support to data. They employed the FDMA, where each user was allocated in a channel during the communication. They were highly affected by the coverage limit and their performance did not meet expectations of many users [2]. The used signal was the AMPS, it did not presented amplitude modulation, and thus, the PA had not the low efficiency problem due to PAPR [10].

The second generation (2G) was based on the GSM signal that emerged around 1991. It employed a reliable digital technology to send voice and data with a time division multiple access (TDMA) scheme where users could share the same channel or the code division multiple access (CDMA), where one codification is assigned to each user during the call time. The original GSM has constant envelope, thus, it does not presents problems with the PAPR.

However, the standard Evolved Data for the GSM Evolution (EDGE) adopted an 8 PSK modulation with 3 bits/symbol, which needs a complex filtering that produces at the end a PAPR of 3.2 dB (due only to the filtering, not to the 8 PSK constellation [10]) which started the reduction of mean efficiency on conventional PAs.

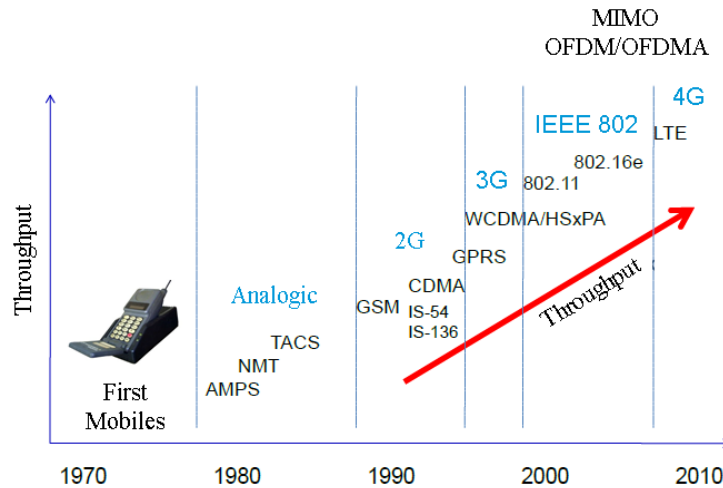


Figure 3.1 – Wireless communication system evolution

The third generation 3G (year 2000) began with the Universal Mobile Telephony Service (UMTS) that uses QAM modulation. It presents support to multimedia and data transfer rates from 384Kbps to many Mbps. This generation presents reliability in the access to 2G networks and in some cases the 1G. It is based on TDMA, some variations of CDMA and wideband CDMA (WCDMA). Due to amplitude modulation and high PAPR which produces a signal with probability distribution function (PDF) concentrated on the backoff (3G signal PDF [10] in Figure 3.2), this standard presents the low efficiency problem when used in conventional PAs. Nowadays mobiles normally supports a long time of voice transmission, however, data transmission with 3G standard quickly depletes the battery. The contribution for the PAPR of the UMTS signal comes from the QAM modulation and the root raised cosine filtering [10].

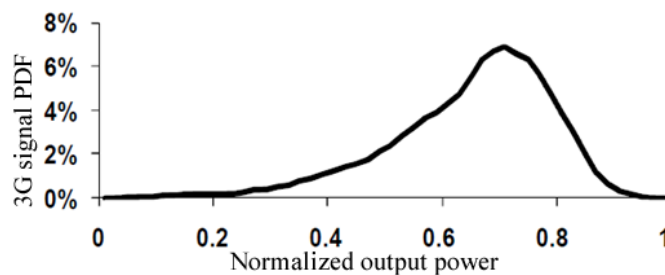


Figure 3.2 – 3G signal PDF (UMTS - WCDMA) [10]

The extension of UMTS, the High Speed Package Access (HSPA), increased the modulation order of the QAM due to produce higher data transfer rates. The PDF of this UMTS upgrade is shown in Figure 3.3; it presents a PAPR from 4.9 to 7.2dB in according to 300 thousand types of signal that can be used [10].

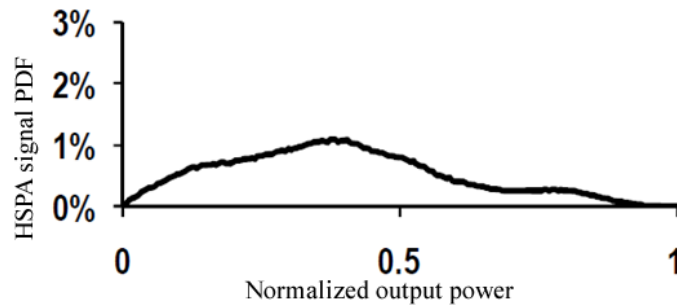


Figure 3.3 – HSPA signal PDF [10]

The fourth generation 4G has been defined since 2010 and today is known by the LTE-Advanced standard. At the downlink it is based on the OFDM and it presents a PAPR around of 12dB and the PDF according to Figure 3.4.

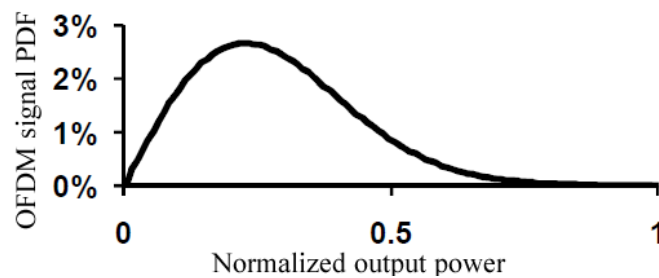


Figure 3.4 – OFDM signal PDF [10].

It is already defined [23] that the 4G must offer support to multiple access in BTS and present data rates higher than 50 Mbps. It must offer IP interoperability for internet access and data exchange between 2G and 3G systems. Its downlink uses the OFDMA with multiples antennas (MIMO) and its uplink uses the SC-FDMA, presenting lower data rates but with lower PAPR helping to mitigate the PAPR problem.

3.2.1 The LTE/LTE-Advanced Standard

The future of the mobile communications market is on the possibility to offer internet services with data rates similar to wired internet. The Long Term Evolution (LTE) standard has been called as 4G by commercial advertisement but it is yet a 3G communication system [24], been considered also as super 3G or 3.9G [25]. One of the main features of the 4G standard are the

data rates greater than 50Mbps [2] and the IP interoperability, which multiple wireless networks are superposed and the connection switch between them is controlled by a higher layer or an integrated intelligence inside the layers: 3G mobile network, wireless LAN, WANS, satellite.

The LTE permits data rates of 100Mbps in the downlink and 50Mbps in the uplink and with cost reduction per Megabit. Its bandwidth is modulated in according to data transfer needs (1.25 – 2.5 – 5 – 10 – 15 or 20 MHz) [25]. The LTE uses recent transmission technologies to permit optimized data rates according to the possibilities of the data transfer point to keep the connection in any geographic localization [25].

The LTE uplink uses the SC-FDMA scheme with 16-QAM as the modulation with higher PAPR (7.03dB [9]) and output power of 23dBm. Its power spectral mask [8] is showed by the Figure 3.5, it is defined in the central frequency and it is dependent of the chosen bandwidth. The main specifications for the LTE and other standards are summarized in Table 3.1 [8].

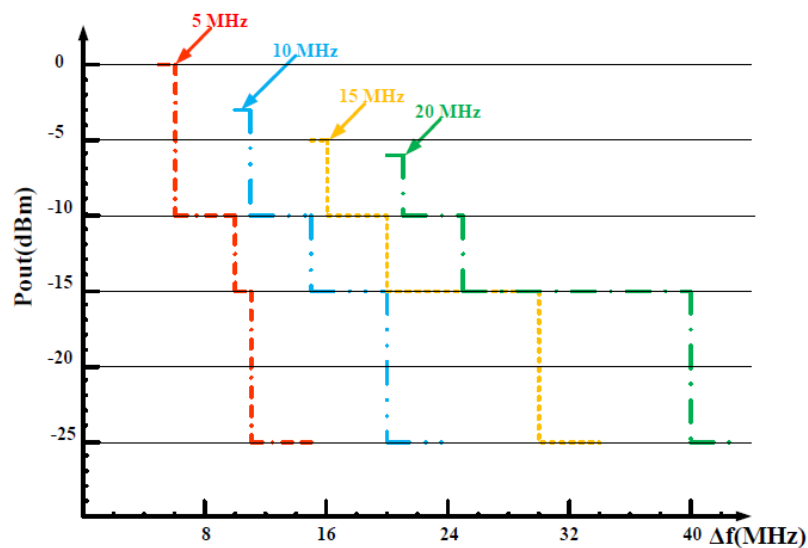


Figure 3.5 – LTE power spectral mask [8].

Table 3.1 – Characteristics of main wireless communication standard systems [6].

Group	Standard	Tx (MHz)	Rx (MHz)	Application	Access Technique	Modulation	Data Rate		
WLAN	WiFi	IEEE 802.11a	5150-5350		Data	OFDM	OFDM, BPSK, QPSK, 16QAM, 64QAM	54 Mbit/s	
		IEEE 802.11b	2412-2472		Data	DSSS	DQPSK, DBPSK, CCK	11 Mbit/s	
		IEEE 802.11g	2412-2472		Data	OFDM	OFDM, BPSK, QPSK, 16QAM, 64QAM	54 Mbit/s	
	IEEE 802.11ac	5180-5825		Data	SDMA	64QAM, 256QAM	500 Mbit/s		
Mobile	GSM	GSM900	880-915	925-960	Voice	TDMA	GMSK	14.5 kbit/s	
		DCS1800	1710-1785	1805-1880	Voice			115 kbit/s	
		PCS1900	1850-1910	1930-1990	Voice				
	EDGE	1710-1785	1805-1880	Data	TDMA, FDMA	GMSK, 8PSK	384 kbit/s		
	UMTS		1920-1980	2110-2170	Data	W-CDMA	QPSK, HPSK	2 Mbit/s	
					Image				
					Voice				
	WiMAX	2000-11000		Data	TDMA, OFDMA	BPSK, QPSK, xQAM	70 Mbit/s		
	LTE	Brazil	2500-2570	2620-2690		Data	OFDMA (DL)	QPSK, 16QAM, 64QAM	100 Mbit/s
			USA	700-716	728-746				
Asia		1710-1785	2110-2155						
		815-845	860-890						
		1850-1910	1930-1990						
Europe	2500-2570	2620-2690	2620-2690	Voice	SC-FDMA (UL)	50 Mbit/s			
	791-821	832-862							

3.2.2 The OFDMA and the SC-FDMA

The OFDMA is derived from the OFDM which corresponds to a robust communication wireless scheme for variant channels. The OFDMA presents good performance in the presence of multipath due to its multi-tone carriers (Figure 3.6) and cyclic prefix (helps synchronization and mitigates inter symbol interference). It is used in all new standards, including the 802.11a,g, draft 802.11ac, 802.16d,e, 802.22, DVB-T, DVB-H, DAB. The LTE was the first standard of 3GPP that adopted the OFDM.

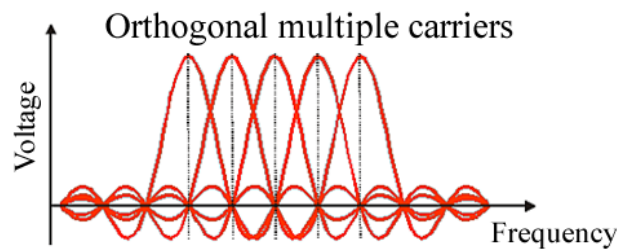


Figure 3.6 – Multiple orthogonal carriers in OFDM.

The OFDM is robust because it transforms time and frequency variant channels in flat channels, eliminating the need of a complex equalization. In the case of frequency variant channels, they became flat for the OFDM due to its narrow band sub-carriers (Figure 3.7).

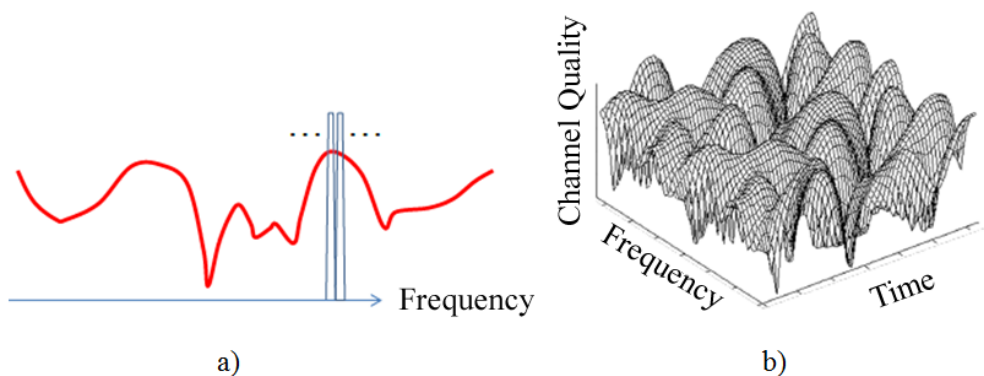


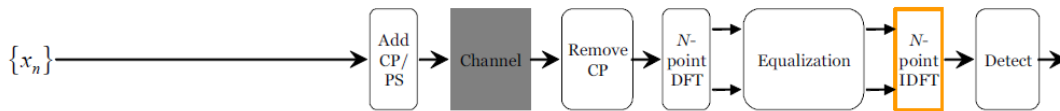
Figure 3.7 – a) Frequency variant channel seen as flat channel by the OFDM. b) Example of frequency and time variant channel.

The OFDM and the OFDMA work separating a fast signal in many slow subcarriers which optimizes the communication robustness. These subcarriers can transmit the information without been subjected to multipath distortion. The OFDMA is the multi user version of the OFDM; it is capable to dynamically assign subcarriers subgroups to individual users using the TDMA and the FDMA. The OFDMA supports simultaneous multiple users, been a point-to-multipoint scheme, the OFDM is point-to-point scheme.

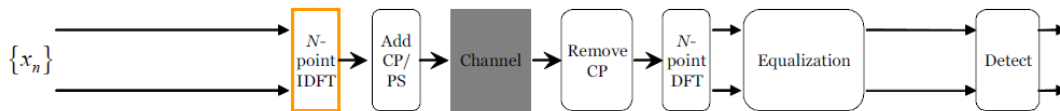
The SC-FDMA is an extension of the SC/FDE (single carrier with frequency domains equalization) that accommodates the multi user capability [26] [27]. The SC/FDE is used to mitigate the frequency selectivity effects in a channel. It provides a similar performance to the OFDM (even for a channel with long delay [26] [27]) with essentially the same complexity.

The Figure 3.8 presents the SC/FDE block diagram and compares it to the OFDM. It is possible to observe that both schemes use the same communication blocks and that the only difference is the localization of the IDFT block (Inverse Discrete Fourier Transform). According to that characteristic, the SC/FDE has a performance similar in spectral efficiency [26] [27]. Beyond the similar structure, the SC/FDE has advantages over the OFDM, as for example, less PAPR due to de single carrier modulation, more robustness against spectral null, low sensitivity to frequency offset and less complexity in the transmitter, which is an advantage to the mobile.

SC/FDE



OFDM



* CP: Cyclic Prefix, PS: Pulse Shaping

Figure 3.8 – The SC/FDE and the OFDM [28].

According to the block diagram of the SC-FDMA system (Figure 3.9), it can be seen as an OFDMA with a spread DFT or a coded DFT, where symbols in the time domain are transformed to the frequency domain by a DFT before getting into the OFDMA modulation [29]. Other similarity between then includes the modulation and the data processing based in blocks, transmission band division in narrow sub-bands, equalization process in the frequency domain and the use of cyclic prefix. Their differences are basically the data detection realized

by the OFDMA in sub groups of sub-carriers and the detection after an additional IDFT on the SC-FDMA.

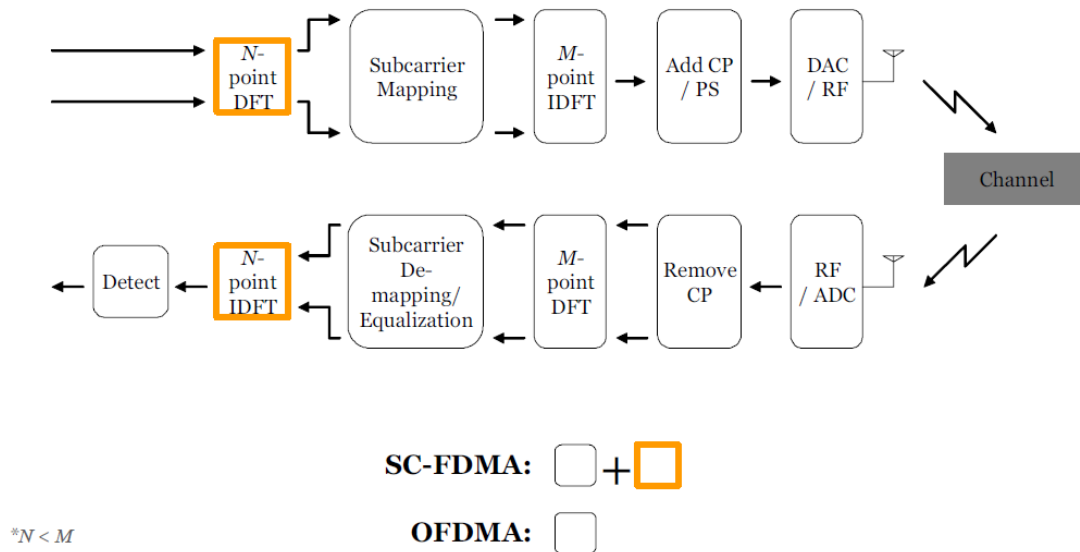


Figure 3.9 – Block diagram of the SC-FDMA system

3.3 THE CMOS TECHNOLOGY

The main motivation on the development of silicon based technologies is the low cost capability due to the abundance of material on the planet and the objective to reach a huge number of consumers. Beyond the low cost, it is a well suited technology for miniaturization. Its evolution follows the transistor channel length reduction (350nm -> 180nm -> 130nm -> 65nm -> 45nm -> 32nm -> 28nm) which increases the frequency of operation allowing the production of faster digital circuits. The miniaturization also permits the integration of whole systems in a single chip, which is called SoC (System on Chip). This integration increases the device reliability and reduces costs by the elimination components on the PCB and by reducing the used area. Beyond the many advantages of the CMOS technologies there are also many constraints that challenges the designer (Annex B) as parasites and low supported voltage, so a special attention must be done on the reliability of the design.

Many digital and RF blocks have been already successfully integrated in the same chip. However, for mobile applications, the PA continues to be a block that is implemented apart from the others [8]. The Figure 3.10 presents the PCB of the iPhone 3 from Apple with PAs for WCDMA and GSM applications implemented in separated CIs. Beyond that, normally

integrated PAs are implemented in expensive technologies, as for example, the GaAs due to its better performance of output power and efficiency related to CMOS [8].

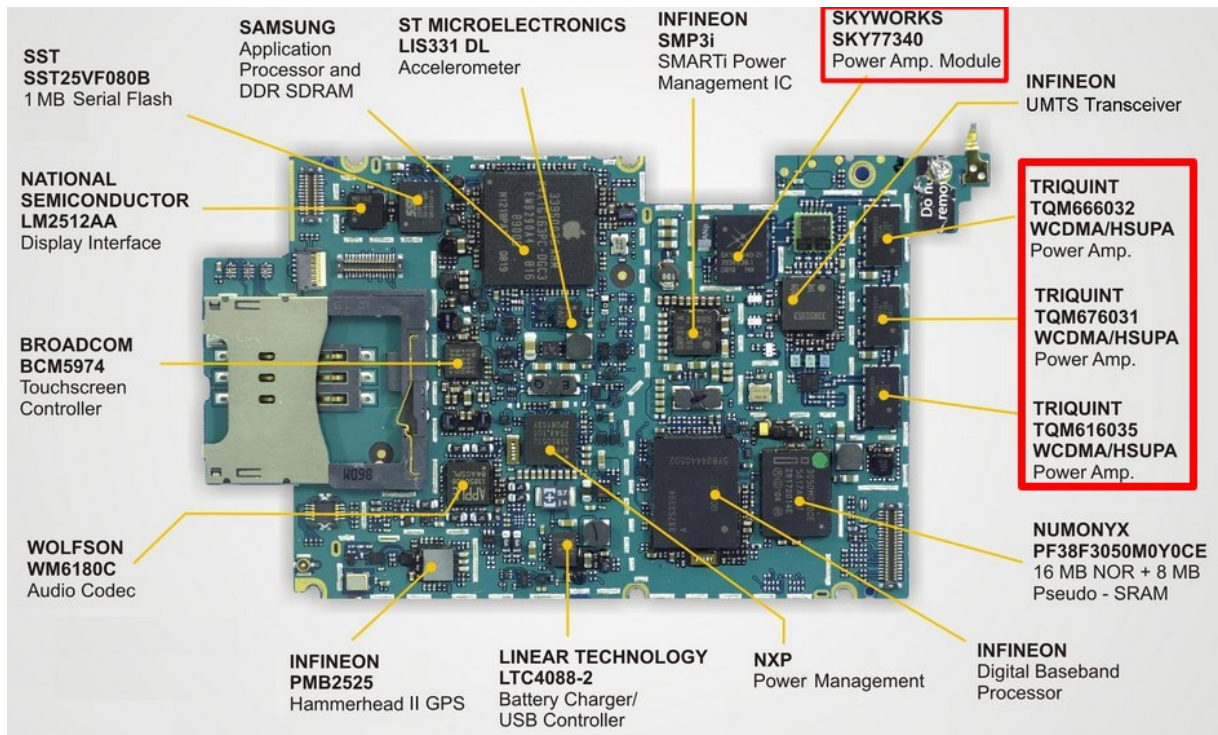


Figure 3.10– iPhone 3 printed circuit board [30].

3.4 CONCLUSIONS

It can be observed that the evolution of the mobile communications, in the point of view of data transmission volume, walks towards the PAPR increasing which reduce the efficiency in the transmission. After observing OFDMA and SC-FDMA characteristics, it can be concluded that the PAPR problem is a challenge for implementing the OFDMA system in mobiles, which induced the application of the SC-FDMA in the 4G uplink to mitigate this problem.

Currently, PAs are not implemented among other integrated circuits of the RF chain in the same chip. Despite the challenges of CMOS 65nm, this technology provides the characteristics required by the market, which is price and integration. Thus, solving design challenges makes this technology the best option for large production.

4 POWER AMPLIFIERS BIBLIOGRAPHIC REVIEW

4.1 INTRODUCTION

In small signal power amplifiers, the input power is sufficiently small to consider the transistor as linear. In these cases, S-parameters are well defined and do not depend on the signal input power or the output load impedance, a fact that hugely simplifies the design of fixed gain and low noise amplifiers. For high input power levels, transistors are no longer linear, and in these cases, impedances seen at the input and at the output start to depend on the input power level, which turns the design into a complex task requiring the use of iterative methods to determine optimal impedances [31], beyond the lack of reliable analytic models to provide precise results to the designer.

This chapter starts with performance parameters used on the PA design. Then, basic structures for signal power amplification and PA classes are presented. The approach becomes more practical with the presentation of the load-pull/source-pull method and the conventional integrated PA's design technique. PA performance enhancement methods are divided in efficiency enhancement and linearization techniques. This work is focused on the efficiency enhancement technique created by Doherty [21]. The chapter presents also a revision on the efficiency techniques, the DPA design method and its bibliographic revision.

4.2 MEASUREMENTS OF POWER, GAIN AND EFFICIENCY IN A PA

Many measurements of power can be observed in a circuit with a PA, as can be seen in the Figure 4.1. The parameters of this simplified schematic can be defined as:

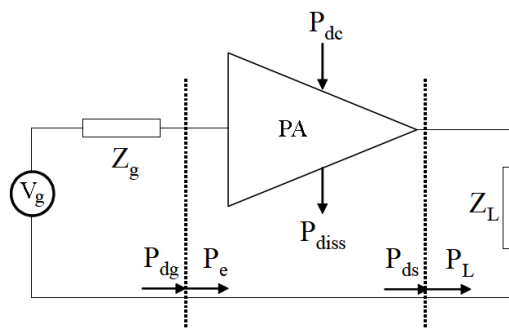


Figure 4.1 – Simplified circuit with a power amplifier [32].

V_g : Generator voltage.

Z_g : Generator impedance.

Z_L : Load seen by the PA.

P_{dg} : Maximum available power in the generator.

P_e or P_{in} : Input power in the PA.

P_{ds} : Maximum available power on the PA output.

P_L or P_{out} : Power provided to the load.

P_{dc} : Power provided by the supply.

P_{diss} : Dissipated power by the PA.

It can be considered that the PA is matched for power gain when $P_{dg}=P_e$ and $P_{ds}=P_L$. However, when there are wave reflections at the PA input and/or output, losses make these equalities to change into $P_{dg}>P_e$ and $P_{ds}>P_L$. With the presented power parameters in Figure 4.1, three types of gain can be defined:

Operational power gain: relation between the provided load power P_L and the power at the input of the PA P_e .

$$G_p = \frac{P_L}{P_e} \quad (1)$$

Available power gain: permits to consider the matching at the input, computed by the relation between the measured power on the PA output (P_{ds}) and the maximum available power at the generator.

$$G_d = \frac{P_{ds}}{P_{dg}} \quad (2)$$

Composite or transconductance gain: approach used for designing a system with a PA because it represents the relation between the load power (P_L) and the available power at the generator (P_{dg}). It is the most used expression on RF and microwave PA design for considering the matching at the input and output. This gain concept was chosen for presenting all analysis in this thesis.

$$G_t = \frac{P_L}{P_{dg}} \quad (3)$$

Two types of efficiency can be defined in a PA. In PAs with field effect transistors, it is defined the drain efficiency (η) that is the relation between the output power in the load P_L and the DC power provided by the supply P_{dc} :

$$\eta = \frac{P_L}{P_{dc}} \quad (4)$$

The most used efficiency measure in a PA is the Power Added-Efficiency (PAE) [1] [33] [34] [35] which consider the input power on the circuit on the efficiency measurement. With this concept, when the transconductance gain increases, the PAE tends to be equal to the drain efficiency.

$$PAE = \frac{P_L - P_{dg}}{P_{dc}} \text{ or } PAE = \eta \left(1 - \frac{1}{G_t}\right) \quad (5)$$

The graph in Figure 4.2 represents three main performance curves analyzed in a PA: the gain (G_t or G), the output power (P_L or P_{out}) and the PAE.

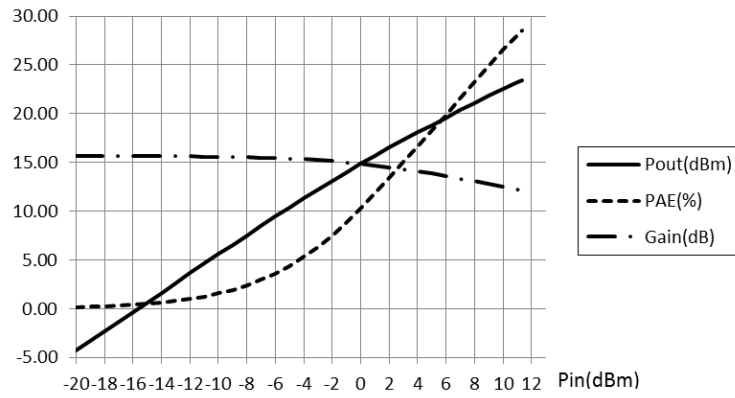


Figure 4.2 – Main performance parameters in a PA.

4.3 LINEARITY MEASUREMENTS

The first measurement regarding to the PA linearity is the 1dB compression/expansion point (P_{1dB}) which can be determined by the PA output power or gain performance in relation to the input power. On a linear PA, the gain performance starts with a horizontal shape, as can be seen in Figure 4.3. The point where the curve leaves its horizontal line, reaching +1dB or -1dB, is considered as the expansion or compression 1dB point, respectively. The PA is considered linear until this point, after it there is enough amplitude distortion (AM/AM distortion) to consider it as non-linear.

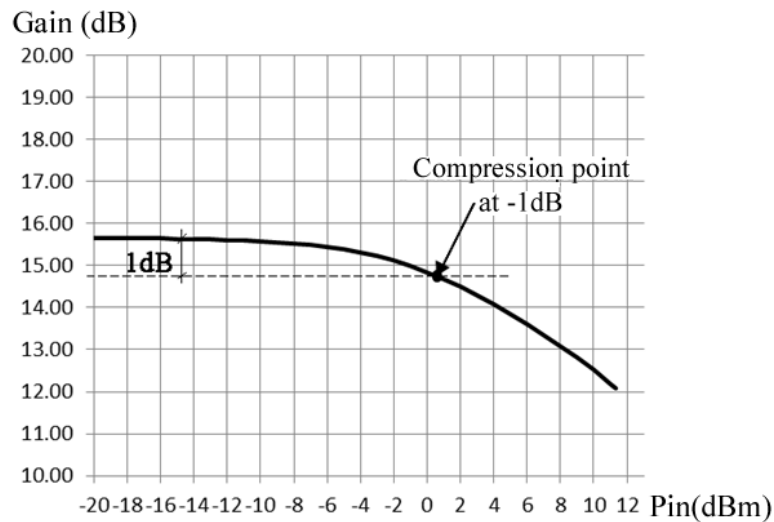


Figure 4.3 – Compression point at -1dB seen by the gain performance.

Other way to measure this distortion point is by regarding the output power curve in relation to the input power (Figure 4.4). The compression point is found when the PA output power performance moves 1dB away from the linear extension of its initial output power curve. The output power value at this point is defined as OCP1 (fundamental output compression point) and the input power value is defined as ICP1 (fundamental input compression point).

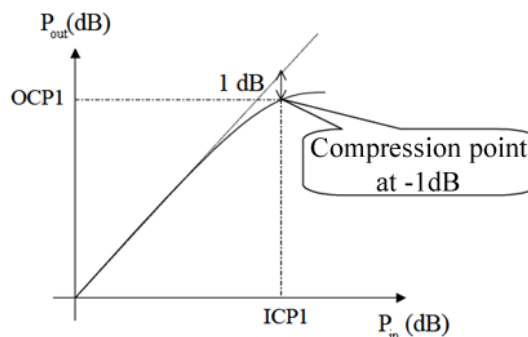


Figure 4.4 – Compression point at -1dB [32].

Beyond the amplitude distortion, there is the phase distortion (AM/PM) that is computed by the output signal phase variation in relation to the input signal phase as the PA input power is increased (Figure 4.5).

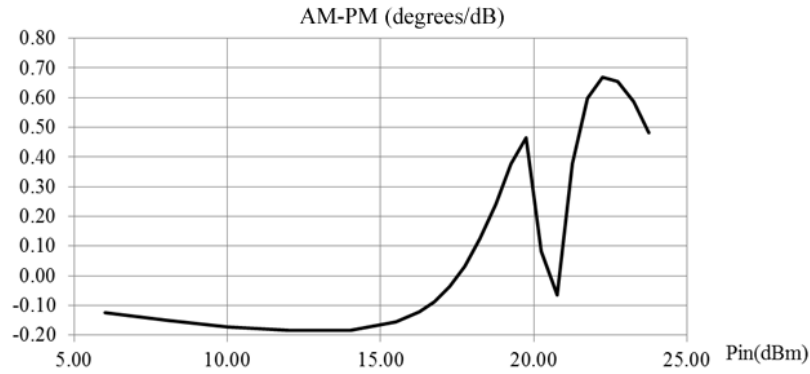


Figure 4.5 – Phase distortion or AM/PM distortion

The AM/AM and AM/PM distortion can be measured with the circuit excited by only one frequency. Other important linearity measure for slightly non-linear systems is the third order intercept point IIP3 (Figure 4.6) which needs the excitation of the circuit with two frequencies (f_1 and f_2). The IIP3 measures the distortion caused by the third order intermodulation products ($2f_1-f_2$ and $2f_2-f_1$) due to non-linearities in active devices [32]. This point can be found by the intersection of the fundamental output power curve and the third order product component. The IIP3 can be approximated computed using equation (6) [36]:

$$IIP3_{dBm} - ICP1_{dBm} = 9.6dB \quad (6)$$

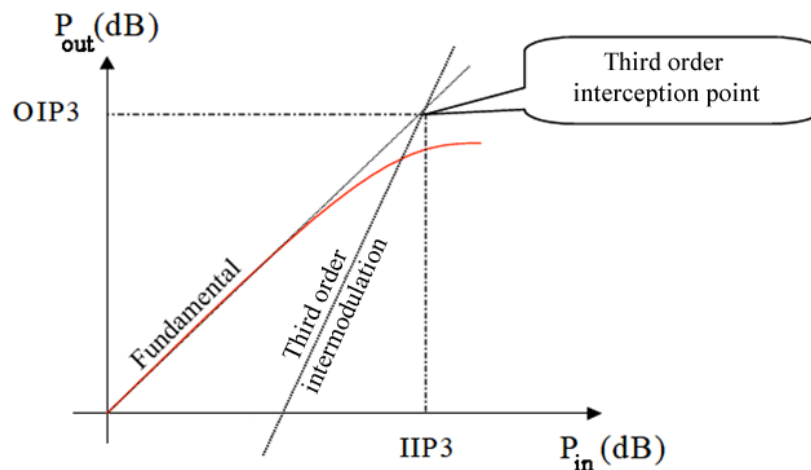


Figure 4.6 – Third order interception point [32].

The Adjacent Channel Power Ratio (ACPR) or Adjacent Channel Leakage Power Ratio (ACLR) is another important linearity performance measure for avoiding signal interference. This measurement is computed by the difference between the usable signal power and the

adjacent channel power in dB, as can be seen in (Figure 4.7). The ACLR can be computed by equation (7) (parameters depicted on Figure 4.8 [8]).

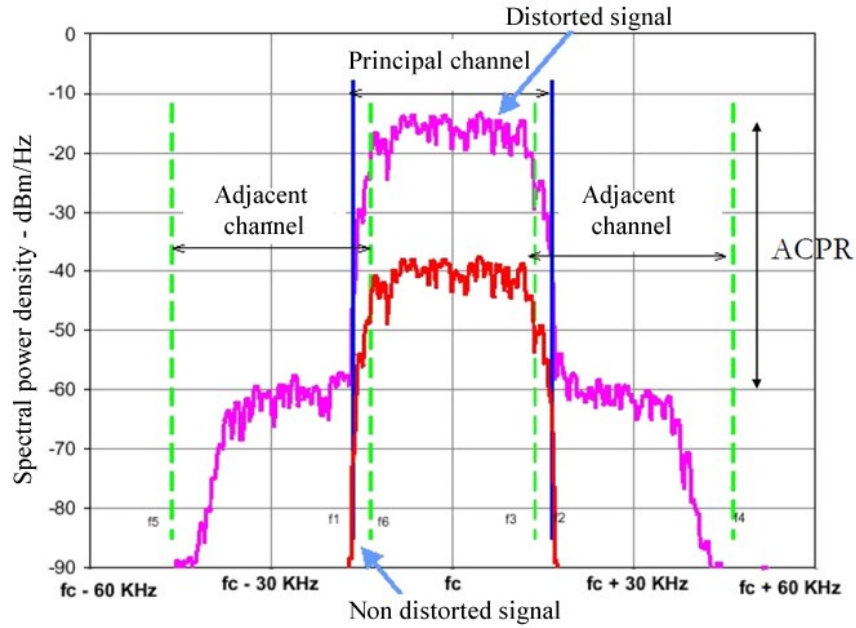


Figure 4.7 – Distorted modulated signal spectrum provided by a non-linear PA [32].

$$ACLR[dB] = 10 \log \frac{\int_{f_c - \frac{B_2}{2}}^{f_c + \frac{B_2}{2}} S(f) \cdot df}{\int_{f_c - \Delta f + \frac{B_1}{2}}^{f_c - \Delta f + \frac{B_1}{2}} S(f) \cdot df} \quad (7)$$

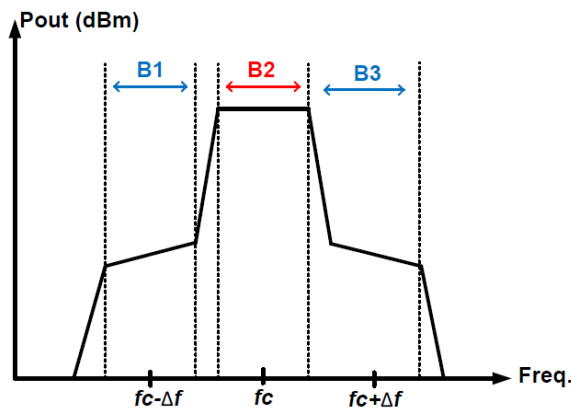


Figure 4.8 – ACLR mask

4.4 PAPR PROBLEM ANALYSIS ON THE PA

The PAPR is defined as the relation between the signal maximum power (P_{max}) and its average power (P_{med}). For an $s(t)$ signal inside a period T , the PAPR expression is defined as (8):

$$PAPR = \frac{P_{max}}{P_{med}} = \frac{\max_{[0,T]} |s(t)|^2}{\frac{1}{T} \int_0^T |s(t)|^2 dt} \quad (8)$$

Conventional PA presents a maximum PAE performance only on the maximum input/output power level. As this power decreases [1] the PAE sharply falls down as can be seen in Figure 4.9.

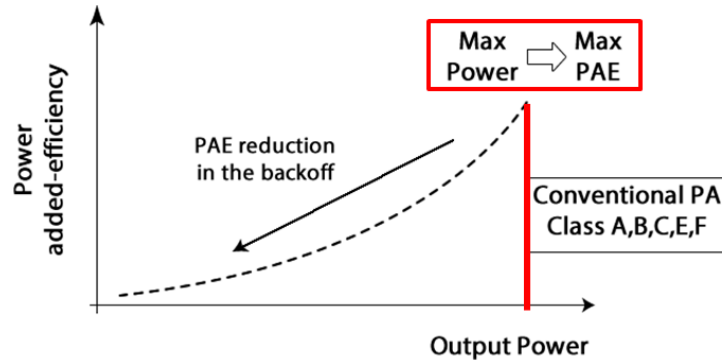


Figure 4.9 – PAE performance curve from conventional.

Signals with high PAPR values present most of the time low and medium power levels and only reaches the maximum efficiency value (maximum power) occasionally, as can be seen in Figure 4.10. When signals with this characteristic are used in a conventional PA the average PAE value becomes very small even if the PA has a high PAE value on its maximum output power level.

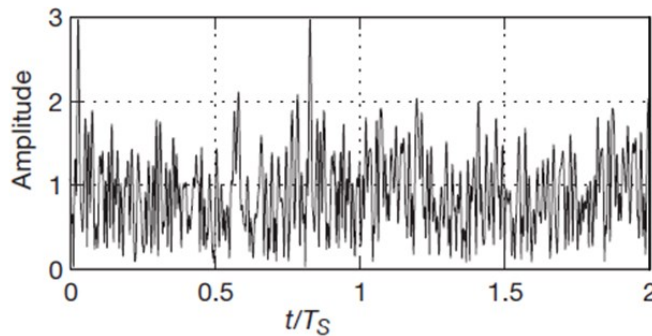


Figure 4.10 – OFDM signal in time domain.

The Figure 4.11 [37] presents probability distribution function of the WiMAX signal and the PAE performance of three types of DPAs and an ideal class B PA. The power distribution curve demonstrates that the signal demand on the maximum output power is only 10% and the demand of the signal in a 7dB backoff is of 70%. The graph also shows the PAE of an ideal class B PA that presents a maximum PAE on a poorly required region (maximum output power) and that it losses 40% of its maximum efficiency on the most required region (7dB

backoff). This illustrates the main objective of the DPA which is to increase the PAE levels where the output power is really required, hence, increasing the PA overall efficiency.

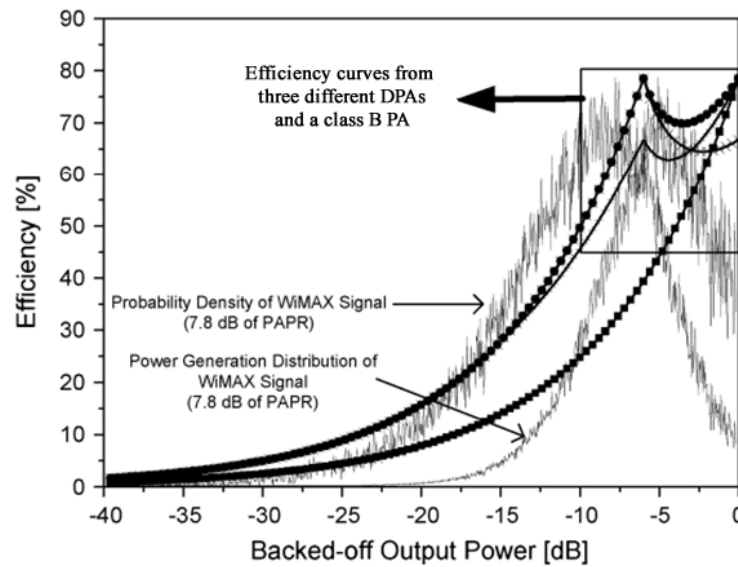


Figure 4.11 – Ideal efficiencies for class B and Doherty PAs and the PDF of a WiMAX signal with 7.8dB PAPR [37].

4.5 POWER AMPLIFIER CELLS

4.5.1 Common-Source Topology and Integrated Choke Inductances Details

There are four basic topologies on the PA design: common source (CS) (Figure 4.12), cascode (Figure 4.13), differential (Figure 4.14) and differential cascode (Figure 4.15) [38] [39] [40]. Other topologies presents some variations, as for example, the SFDS [25] where the input signal is connected on the gate of both transistors on a cascode topology, and the cross-over cascode differential topology [3], where the polarization of the common gate (CG) transistors comes from the drain of the transistors in opposed cycle of operation.

The CS topology is the simplest topology to design; it has few components and needs a small area. With only one transistor, this topology presents lower output powers in relation to other topologies and it also presents a higher coupling of impedance effects between output and input. This means that its input optimal load matching depends on the load seen by the transistor's output, and its output optimal load matching depends on the load seen by the input of the transistor. The optimal impedances also depend on the input power, on the transistor's size, on the polarization and on the choke inductance in the drain (RFC in Figure 4.12).

The choke inductance (RFC in Figure 4.12) is used to supply the circuit with DC current and to block the RF signal. This inductor is designed to present a high impedance level to the signal, normally 10 times greater than the path towards the load. Ideally, the choke inductor must completely block the RF signal and conduct only DC.

Integrated inductors with high inductance values normally present low quality factors ($Q = \omega L/R$). As the number of turns increases (path length) and as the path width decreases, higher is the inductance and the resistance value of the inductor. Increasing the diameter and path width, and reducing the number of turns, the inductance and resistance values of the inductor decrease. The quality factor can be intuitively predicted by this simple rules, but it can only be precisely determined by and electromagnetic simulation because this factor also depends on the topology, path thickness, distance between paths, parasitic capacitances with the substrate and the conductor material.

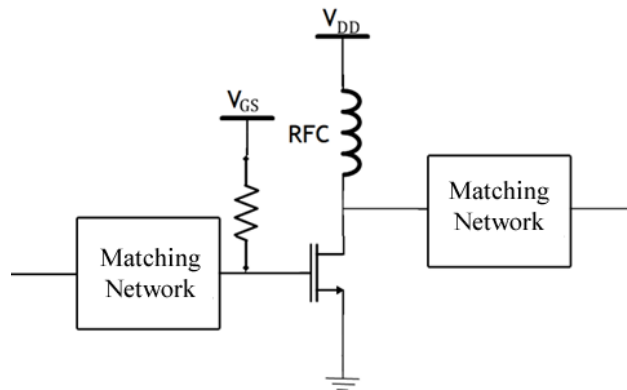


Figure 4.12 – Common source topology

4.5.2 Cascode Topology

The cascode topology presents better isolation in relation to impedance effects at the input and the output. By stacking transistors, it is possible to provide higher supply voltage levels V_{DD} due to produce higher output power levels.

By dividing equally the voltage swing between the cascode transistors, it is possible to considerably increase the V_{DD} to produce higher output power levels without damaging the device. In a cascode topology the voltage swing can also be unequally divided between the CS and the CG transistor, which can lead to higher PAE performance levels.

The voltage swing can be controlled by the voltage applied on the gate of the CG transistor and by a capacitor connected on this same point. Smaller capacitors increase the signal amplitude on the CS transistor and larger capacitors increase the signal amplitude on the CG transistor. Normally, the gate bias of the CG transistor is always higher than the gate bias of CS transistor. Many implementations of the cascode transistor connect the gate of the CG transistor directly on the VDD, which gives priority to the gain and linearity performance of the PA. By polarizing this gate above the VDD it is possible to reach higher PAE levels.

The cascode PA design is more complex than the CS PA due to the increase on the number of components and the interdependence of the optimal impedance over these components, as the transistor's sizes, the polarization, the choke inductance and the capacitor at the CG transistor.

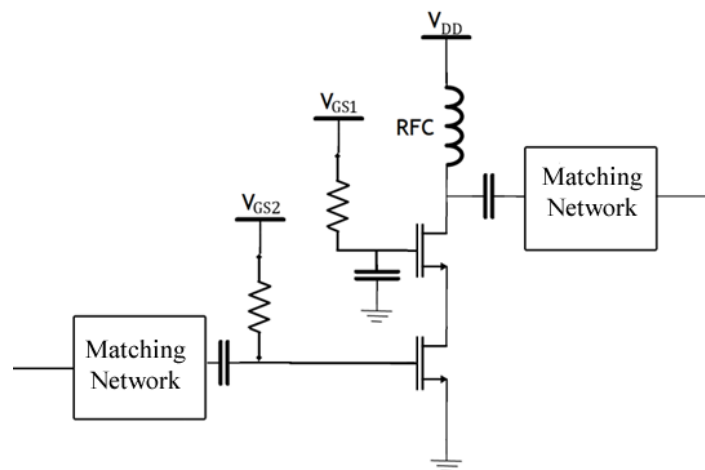


Figure 4.13 – Cascode topology

4.5.3 Differential Topology

The differential topology (Figure 4.14) permits to increase the output power of the PA in relation to the single ended CS topology. The complexity of the differential topology design is on the baluns at the PA input and output. These baluns have many functions as signal splitting or combining, electric isolation and impedance matching.

The impedance matching on baluns (Figure 4.14) is done by a group of capacitors connected in parallel to its windings. Normally the designer's objective is to optimize a balun until it reaches losses less than 1dB. The balun also needs to support the PA current (path width) and to realize a good impedance matching.

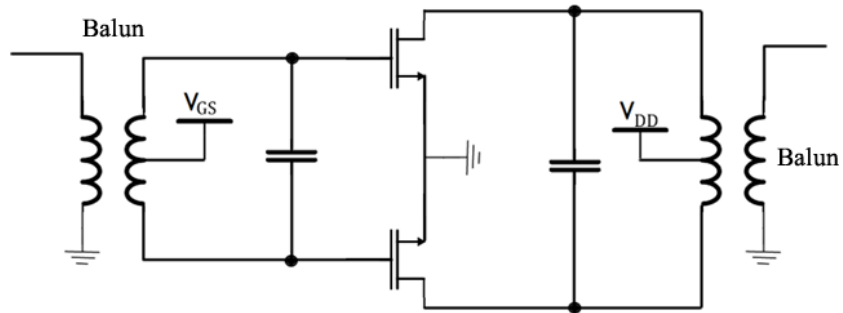


Figure 4.14 – Differential topology

The differential cascode topology is the structure that provides more output power in relation to the other topologies, however, it is the more complex structure to design and that needs more chip area. It is composed basically by two cascode amplifiers, two baluns and it provides 3dB more output power than the single ended cascode topology. For reaching an output power greater than this structure, the solution is the use of voltage or current combination techniques with integrated transformers by the combinations of many power cells in parallel [41].

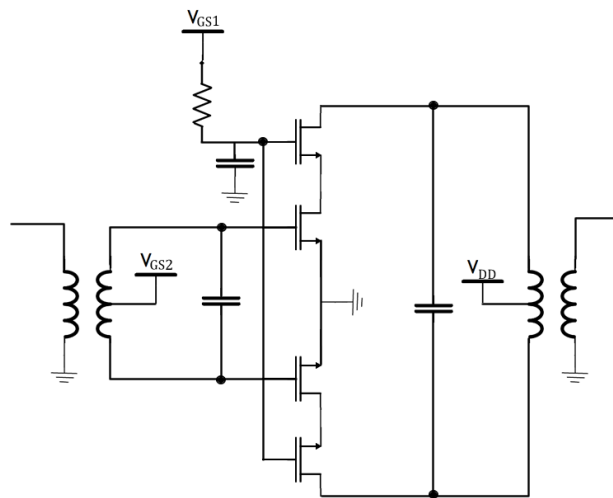


Figure 4.15 – Differential cascode topology

4.6 POWER AMPLIFIER CLASSES

4.6.1 Sinusoidal classes A, B, AB and C

PAs on classes A, B, AB and C belongs to sinusoidal operational classes that are only differentiated from each other by the transistor's conduction angle, which is defined by the bias voltage V_{GS} on the gate of the transistor (Figure 4.16).

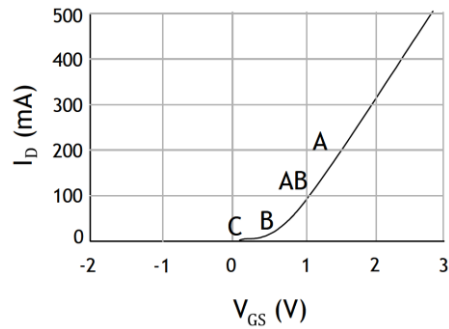


Figure 4.16 – Drain current I_d versus gate voltage V_{gs} .

The conduction angle on class A is 360° , on class B is 180° , on class AB it is between 360° and 180° and the class C is less than 180° . The class A is the most linear class among these sinusoidal classes, the class AB is the class that reaches the higher PAE value been yet linear and the class C is always non-linear. The class B PA is only a concept because in practice the transistors does not starts to conduct abruptly, so there is an intermediary region where it is difficult to define if the PA is on class AB, B or C. The drain current and conduction angle of all this classes can be observed on Figure 4.17.

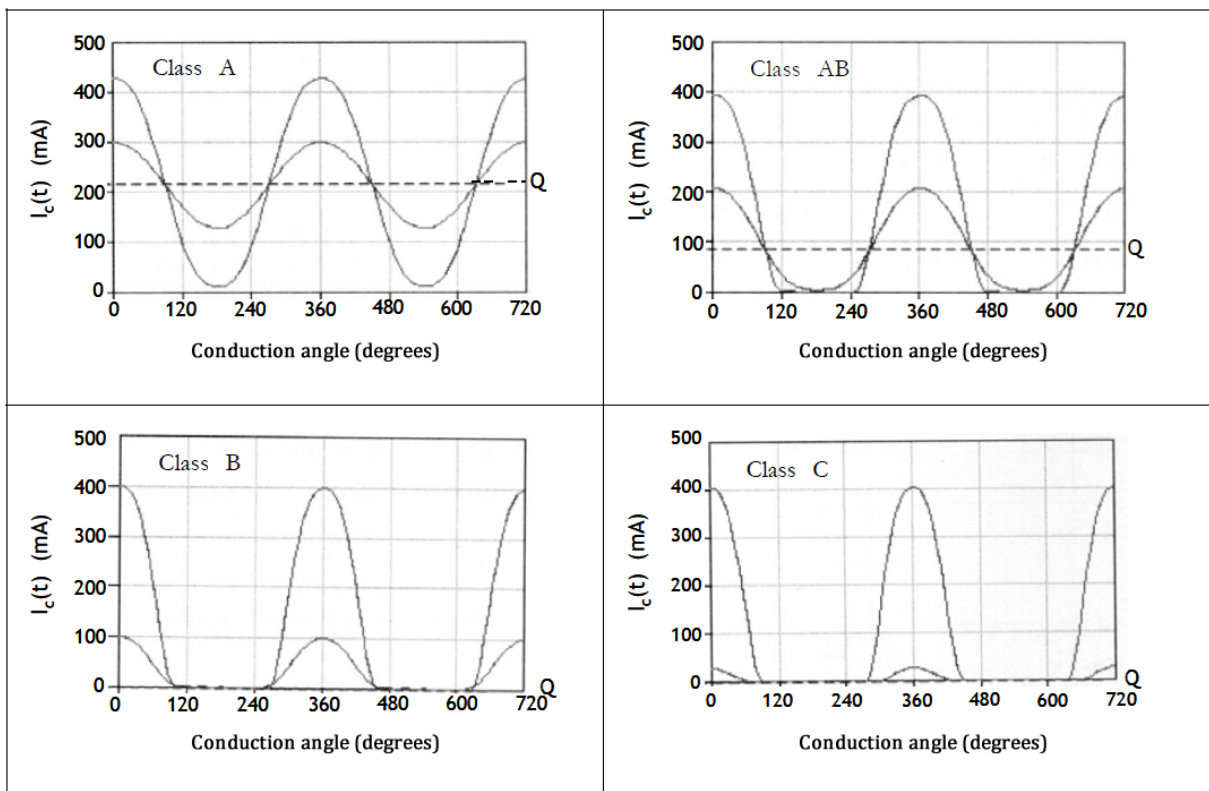


Figure 4.17 – Summary of PAs classes A, AB, B and C [32].

The theoretical maximum efficiency of these amplifiers has already been largely computed and published and can be founded in [1] [32] [34] [4] [42] [5] [43] [44] [38]. The Table 4.1 summarizes the main characteristic of these PAs.

Table 4.1 – PA sinusoidal classes summary

Class	Conduction angle (α)	Maximal theoretical efficiency (η)	Linearity
A	360°	50%	Linear
B	180°	78.50%	Linear
AB	$180^\circ < \alpha < 360^\circ$	$50\% < \eta < 78.5\%$	Linear
C	$< 180^\circ$	$> 78.5\%$	Non-linear

4.6.2 Switching Classes E and F

In class E PAs [38] [44] the transistor works as a switch with two working cycles: open and closed. The transistor is controlled by a square wave voltage at the gate with the objective to permits current flow when there is not drain voltage and to cut the current when there is drain voltage. Ideally, voltage and current at transistor output must have an offset (Figure 4.18) that turns the energy dissipation into zero and the efficiency into 100%.

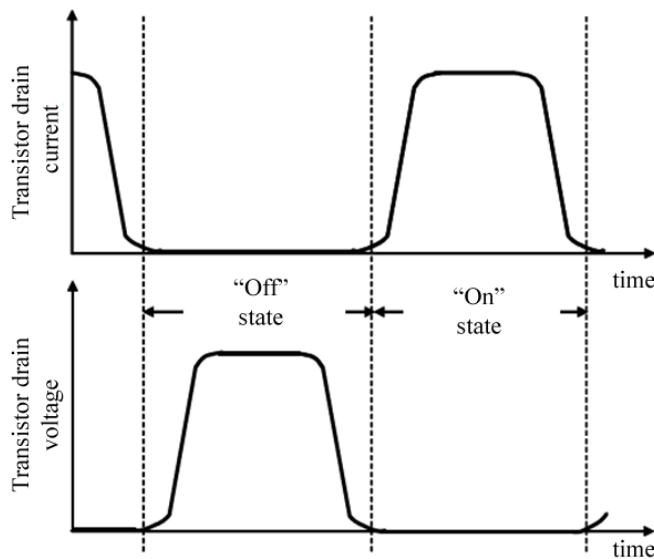


Figure 4.18 – Transistor current and voltage waves in time domain [32].

The basic topology for class E PAs is presented in Figure 4.19. In high frequency this class presents some problems, as for example, the need of high input power and limitation to have a control square wave due to the needed of high harmonic frequency to produce the square shape. The increase of input power reduces the gain and consequently the PAE, which starts to present low values above 1GHz frequencies [32].

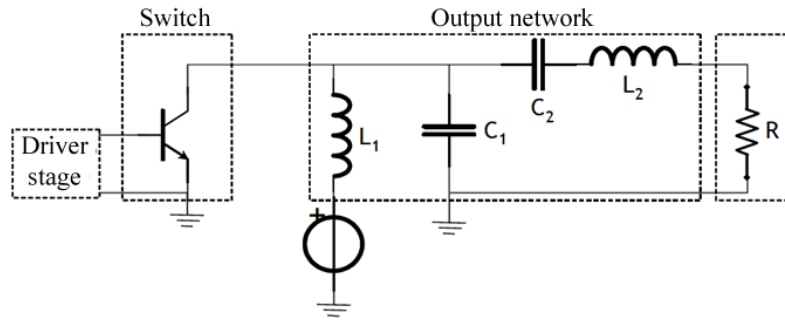


Figure 4.19 – Class E basic topology

The class F [38] [44] (Figure 4.20) consists in creating an approximated square wave voltage by controlling the amplitude of its harmonic components (Figure 4.21). The Fourier series of a square wave presents a fundamental component that is greater than the signal amplitude. As the output power and PAE is computed only with the fundamental component, this PA presents a greater performance than the sinusoidal classes [32]. The Table 4.2 summarizes classes E and F.

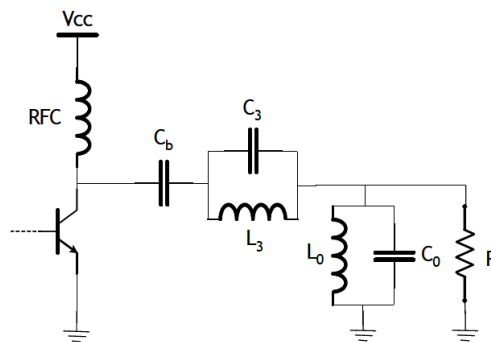


Figure 4.20 – Class F PA topology.

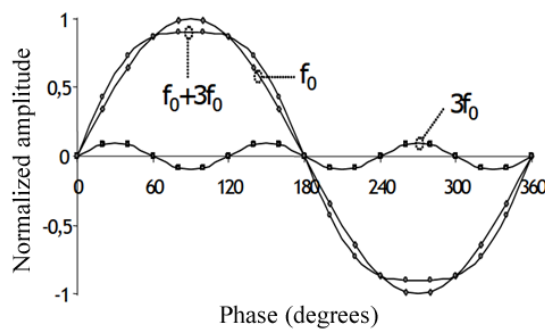


Figure 4.21 – Class F PA signal wave shapes.

Table 4.2 – Class E and F summary.

Class	Input voltage	Output current	Output voltage	Efficiency
E	Square	Square	Square	100%
F	Sinusoidal	Sinusoidal	Square	64%
		1/2 Sinusoidal	Square	100%

4.7 IMPEDANCE MATCHING: LOAD-PULL/SOURCE-PULL METHOD

When the signal wave length becomes small in relation to circuit physical dimensions (high frequency signals), a propagation phenomenon on the electric signal appears, introducing the concept of incident and reflected signal [31]. When this occurs it is necessary to match the impedance between the source, the PA and the load for transferring the maximum power with minimal losses. The source and load impedance normally are known, but, the input and output impedance of the transistor are dependent of too many factors that it is not possible to precisely compute with equations. The determination of these values can be done by the load-pull and source-pull methods.

The load-pull method consists on the test of many different loads on the transistor output for mapping possible performances on the Smith chart. Output power and efficiency performance values are drawn on the Smith chart as level curves and thus, the load that optimizes the output power or the efficiency can be determined. The source-pull method is done in an analog way but on the transistor's input. It can be observed in Figure 4.22 an example of level curves from the load-pull method. These results show that the load that optimizes the output power can be different from the load that optimizes the PAE performance.

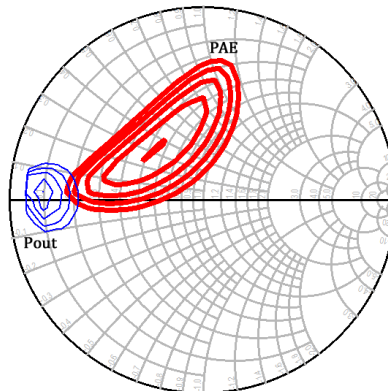


Figure 4.22 – Examples of PAE and output power curves from the load-pull/source-pull methods.

PA transistor's dimensions are normally large which reduce input and output impedances. It is important to observe that optimal input/output loads changes in according to the polarization, frequency, dimensions, technology and input power. The optimal impedance found by these methods is specific for each group of parameters. Another important point is that depending on the PA topology, the load presented on its output changes the optimal impedance of its input and vice-versa.

After choosing all PA parameters, the application of the load-pull/source-pull method is iterative. First an arbitrary load is shown to the transistor input (50 ohm, for example) and then the load-pull method is applied. After determining the optimal output impedance, this optimal value is fixed and the source-pull method is applied to find an optimal input impedance to replace the arbitrary value chosen. After finding the optimal input impedance, the load-pull method is realized again because changing the initial input impedance of 50 ohm to another value will change the result of the load-pull. This cycle is repeated many times. For each input impedance there is a different output optimal impedance, and for each output impedance there is an optimal input impedance. After realizing the load-pull/source-pull cycle sometimes it can be observed that the input and output impedance stops to change, thus, the optimal input/output impedance values converges.

After presenting optimal input and output impedances to the PA, an input power sweep with a Harmonic Balance (HB) simulation is done to plot the PAE, Pout and gain performance from low (-20dBm) to high (20dBm) power levels. Normally, this first loop of load-pull/source-pull is done for an input power that does not correspond to the PAE or Pout peak. If this happens, it is yet possible to increase the PA performance by presenting other impedance values. The designer must choose a parameter to optimize, PAE or Pout, and then keep the input power value that corresponds to the PAE or Pout peak (according to the parameter that he wants to optimize) and put again this value on the source and make again the load-pull/source-pull loop. After some iterations looking for the optimal input power this value converges and then the circuit is considered to have the optimum input and output impedances. This process is shown on the flow diagram in Figure 4.23.

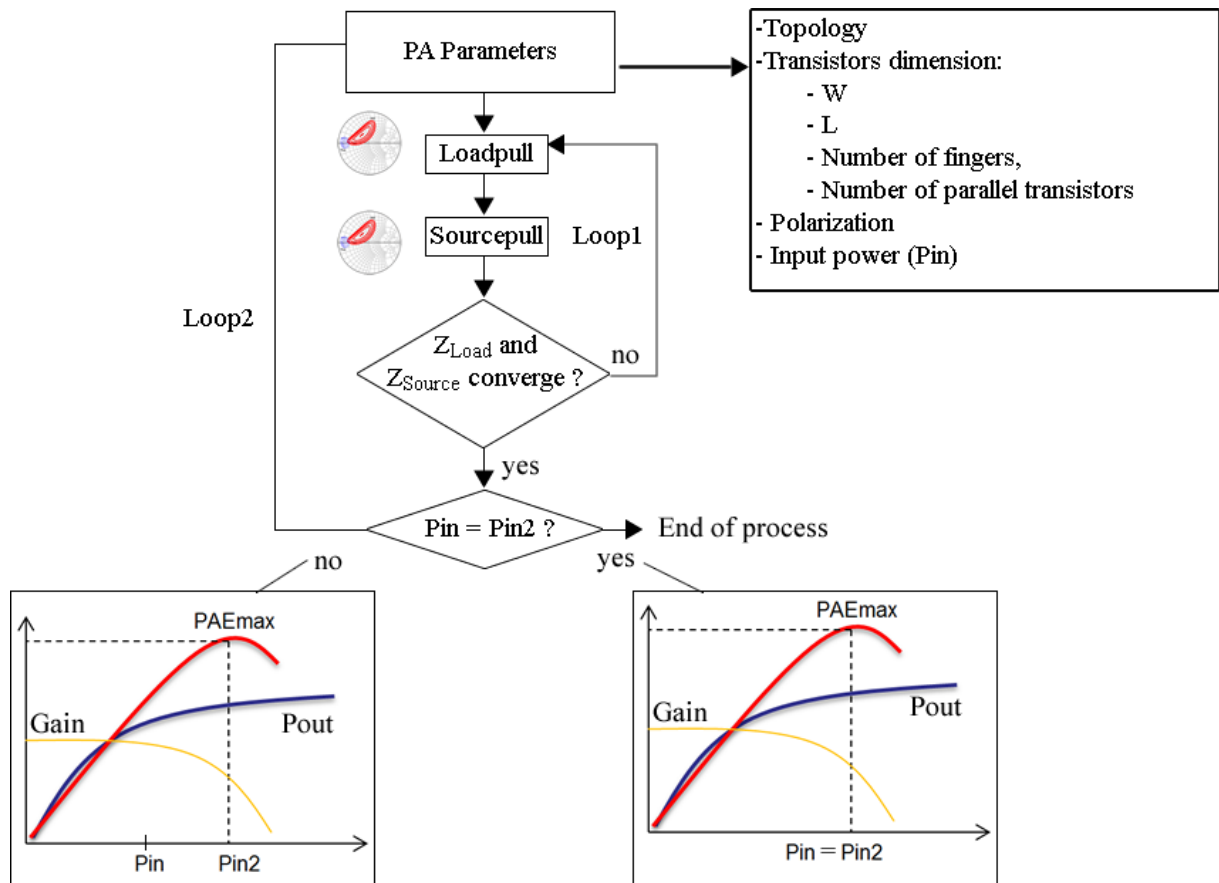


Figure 4.23 – Methodology for determining optimal input and output PA impedances.

The process to determine ideal input/output impedances on a PA is long and hard. There are two loops with an indeterminate number of iterations on the process. During the load-pull and source-pull method there are parameters that must be adjusted, as for example, the search region on the Smith chart, defined by a radius, the center coordinate and the number of points to be simulated. When a region does not cover the maximum PAE/Pout points, the search region on the Smith chart must be redefined. All this process on this work was done on the Agilent Advanced Design System (ADS).

For each point selected on the Smith chart it must be done a HB simulation, which needs the definition of the number of harmonics. It is common to find points which the HB algorithm does not converge, which requires to change the search region until the simulation works. This convergence problem normally appears when the search region is near to the edges of the Smith chart (low impedances) and/or high input power levels are used. For a small number of harmonics, the simulation is faster but with less precision and with more probability of non-convergence. Normally this kind of simulation is done with five harmonics and if the simulation does not converge, this number is increased. For high non-linear circuits more

harmonics are needed to reach the convergence. During this research it was used until 60 harmonics (on single tone simulations) to make some circuits to converge. Thus, beyond the two loops on the input/output impedances determination, load-pull and source-pull process can also be a long process.

4.8 CONVENTIONAL DESIGN METHODOLOGY FOR INTEGRATED POWER AMPLIFIERS

The design of low noise amplifiers (LNA) is well defined by equations and models, however, an increased version [38] of this kind of amplifier for creating a PA is fundamentally unable to produce good results, thus, other design approaches must be considered [38]. The theory of maximum power transfer is of little use to the design of PAs [38]. One of the reasons is that it is not completely clear how to determine the impedances of a non-linear system with large signals [38]. These statements of Thomas H. Lee can be confirmed by the load-pull/source-pull process presented in the previous section. The most important points in the PA design consist on the transistor sizing, polarization and impedance matching. For this problem there is not yet a reliable analytic equation, which imposes the use of an iterative method.

The literature that shows equations for PA performances is vast [38] [39] [40] [4] [1] [32] [5], however, there is a big gap between knowing the shape that PA performances should be and knowledge of how to achieve this result. The conventional design methodology for integrated PAs consists on an iterative procedure of search. The efficiency of this procedure is dependent on designer's experience and its knowledge over the design tools. This task is easier and more direct when the integration technology is mature and well documented.

The Figure 4.24 presents the diagram that describes the initial studies for defining transistors polarization and PA topology. The PA operation class is defined in according to the design objective, which also defines the range of values for its polarization. From the output power specification, the presented flowchart can be followed for determining the required chip area and the PA topology.

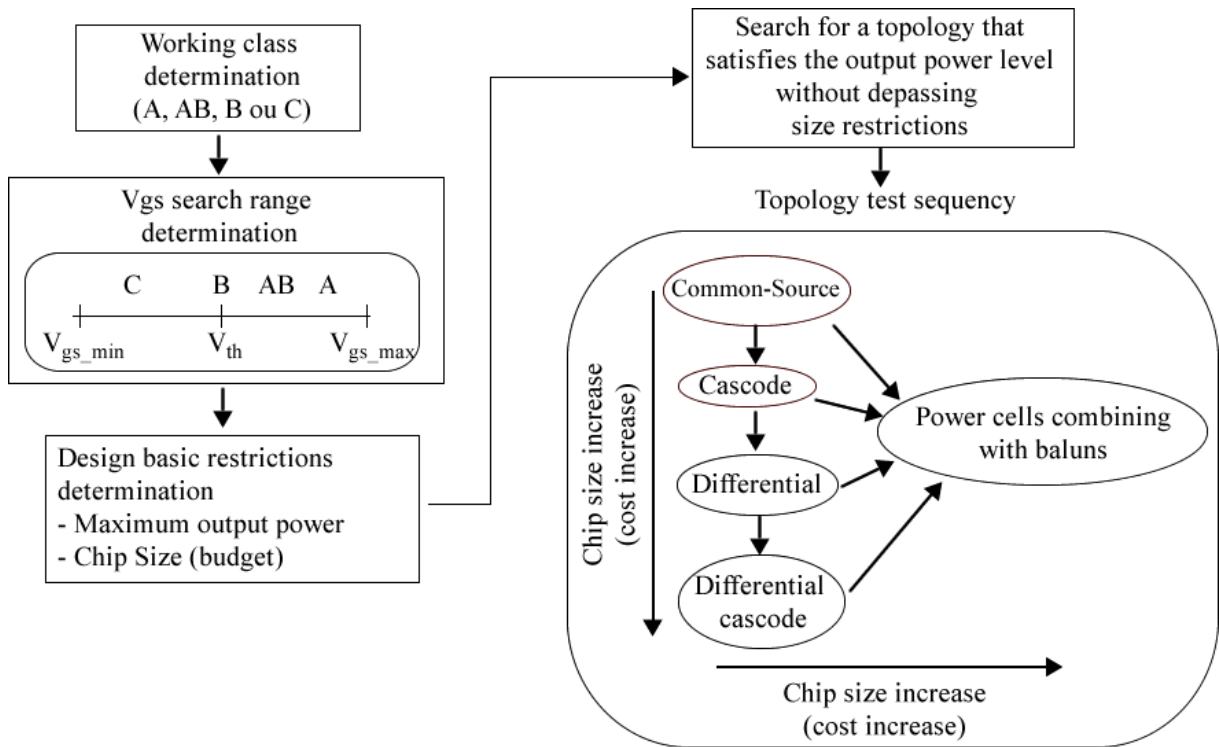


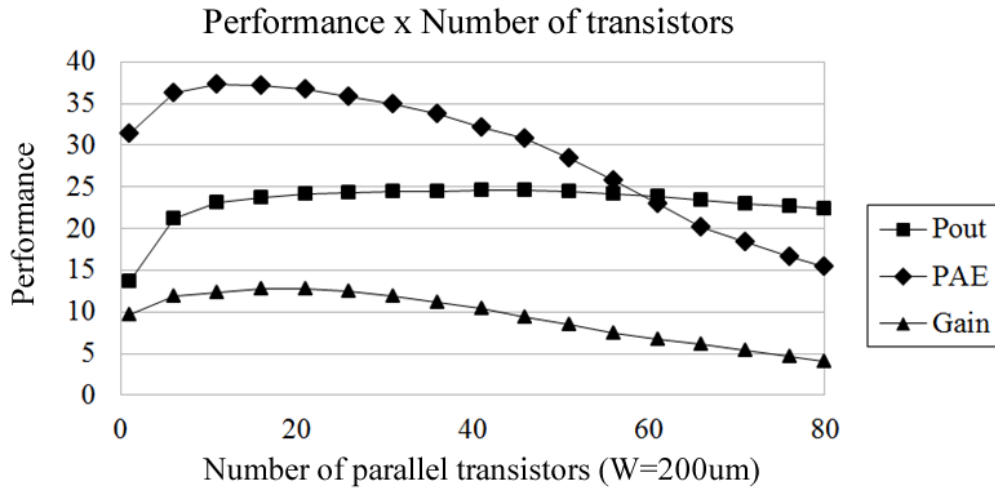
Figure 4.24 – Flowchart for defining PA polarization and topology.

Each topology presents its own particular features. The common-source (CS) topology is simple due to the reduced number of components and bias voltages, however, this topology presents some challenges on the input/output impedances determination. Due to the high interdependence between the input impedance and the output impedance, more load-pull/source-pull loops are required to reach the convergence. Due to the low supported VDD it is not possible to reach a high output power level on this topology.

It is important to note that just increasing transistor's size and the number of parallel transistors is not enough to increase the output power of a PA. Large transistor presents small input and output optimal impedances and high parasitic capacitances. The output power and gain of a PA increases with its W until a determined limit. After this limit, the output power stops to increase and the gain starts to decrease, which also causes the reduction on PAE performance.

The Figure 4.25 presents results of increasing the number of transistors in parallel and its respective P_{out} , gain and PAE performance. It is important to note that for each transistor size and polarization were searched the optimal input/output impedances, so, the decrease of performance shown does not comes from a possible mismatch during the transistor resizing.

For each PA size presented on the Figure 4.25, the ideal impedances were presented directly to the transistor, thus, the figure does not considers losses on impedance matching.



Transistor next25_hvi Cascode Topology, W=200um, Vgs=0.9V (classe AB), VDD=3.7V

Figure 4.25 – Cascode PA Class AB performance study for the number of transistors in parallel.

After an initial study of the PA performance possibilities in relation to its polarization and topology, the project can go to a more realistic stage by regarding all voltage limits and adding the matching networks. The design cycle of an integrated PA passes through schematic, layout and post-layout simulation many times (Figure 4.26).

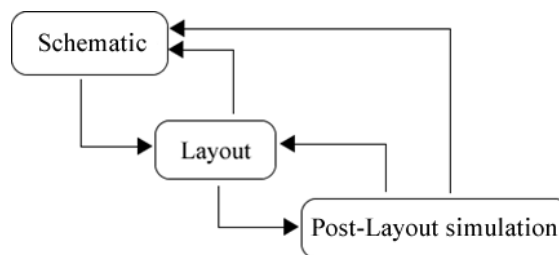


Figure 4.26 – Simplified design cycle for integrated PAs

The Figure 4.27 shows the design cycle for the schematic after the initial study on the transistor possibilities. In according to the working principles of the specific PA, polarizations and transistors dimensions are adjusted and the network matching is done until the circuit present a satisfactory performance with all restrictions respected.

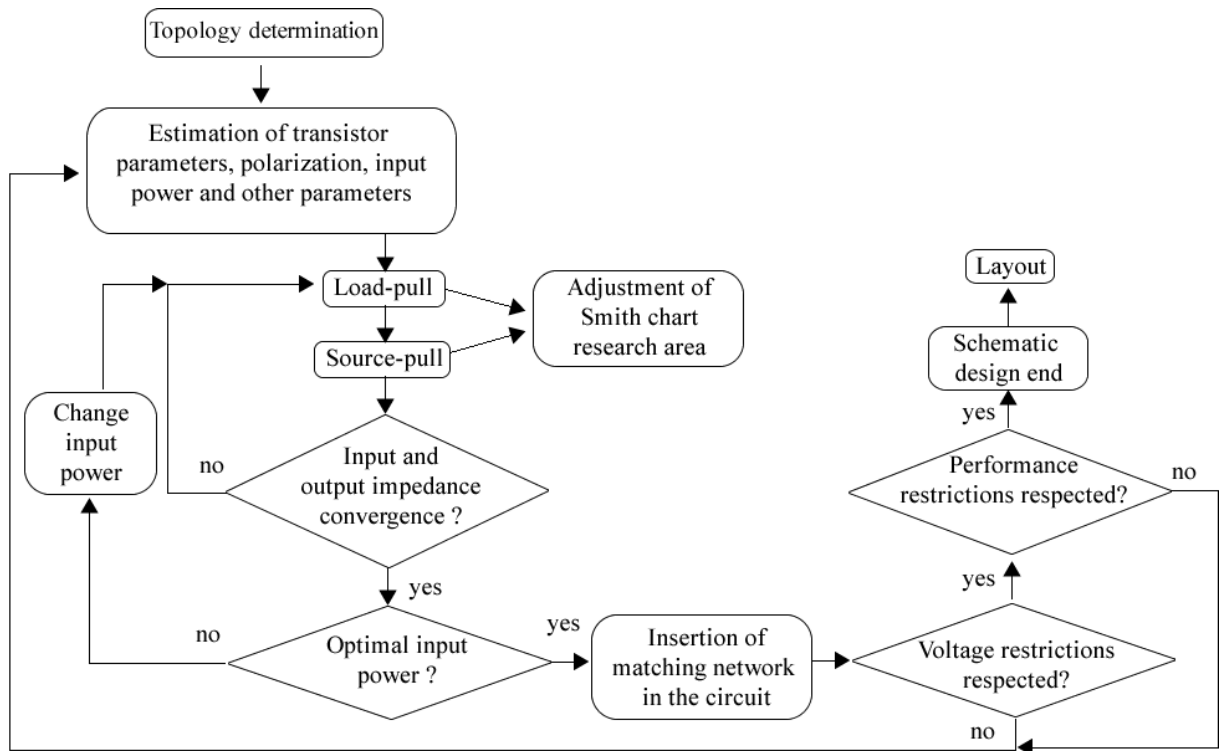


Figure 4.27 – Design cycle of the schematic

The layout design starts when the schematic is ready. At this point some changes can be done on the schematic to make easier the layout, as using an even number of transistors in parallel (which helps the chip symmetry) and changing the number of fingers for supporting the current that will pass through the transistor.

The Figure 4.28 shows the layout design flowchart. During the design, the positioning of each polygon must follow strict rules that are checked by the DRC (Design Rules Check) and the connections made between the components must be equal to the schematic, which are checked by the LVS (Layout Versus Schematic) process. After concluding the layout with success (correct DRC and LVS) and respecting the chip area defined by the budget, the extraction of parasites must be done and then a Post-Layout Simulation (PLS). This simulation shows the parasites impact on the circuit performance. After the PLS it is normal to change the layout or even the schematic to achieve the desired performance.

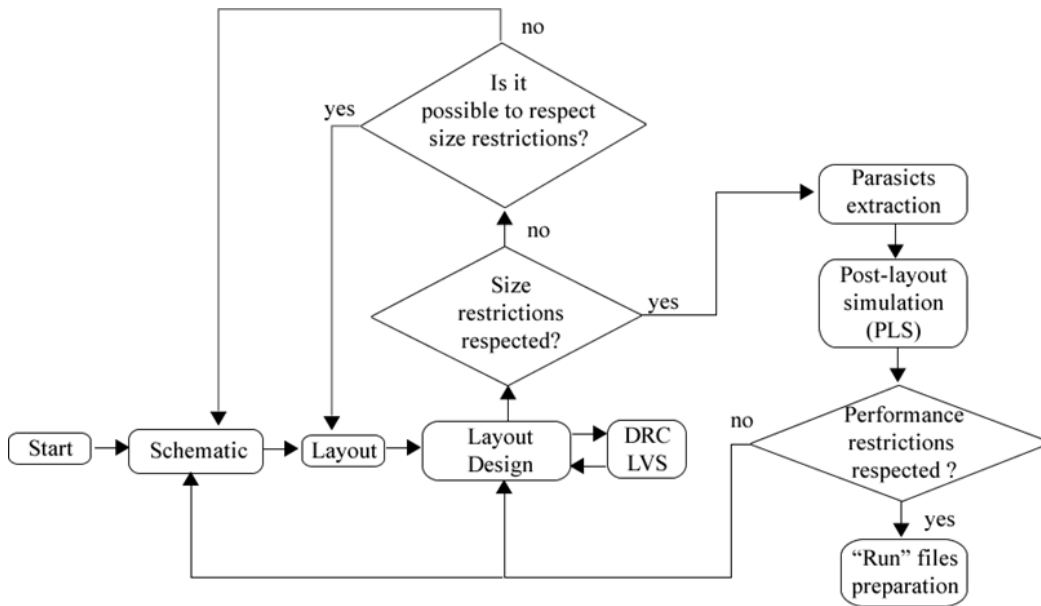


Figure 4.28 – Layout design flowchart

After validating the circuit, final corrections are normally done on the layout to respect final metal density rules (Figure 4.29). To fabricate the chip there are many density rules that must be respected with the risk of the chip being damaged during the fabrication process or even to damage other chips from other designers that are positioned on the same wafer. For respecting the density rules, many blocks of metals (dummies) are spread on the layout without being connected to anything. At the end of these processes an LVS must be done for checking if any block has done any undesired connection in the circuit. Finally, the layout is exported on the GDS format and sent to fabrication.

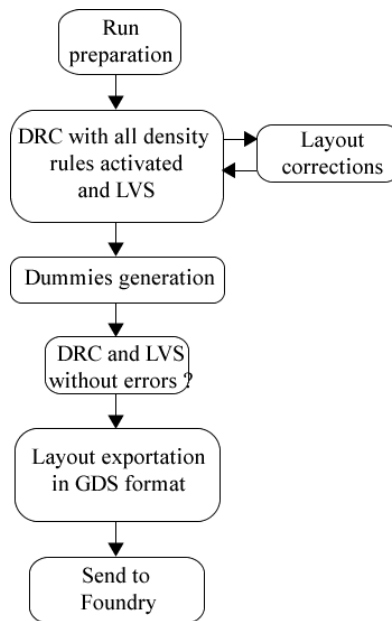


Figure 4.29 – Final process on the chip design

4.9 EFFICIENCY ENHANCEMENT TECHNIQUES

Many techniques have been created with the objective to increase PA efficiency on low/medium power levels. Theoretically, these techniques present a promising performance, however imperfections on the material prevent the performance shown in calculations to get into practice.

The PA efficiency control is basically done by three parameters (Figure 4.30): the polarization current, the supply voltage and the load impedance. The principal challenges on this control are on the consumption of the feedback circuit, the excessive increase of complexity, the increase on chip area and the addition of distortion.

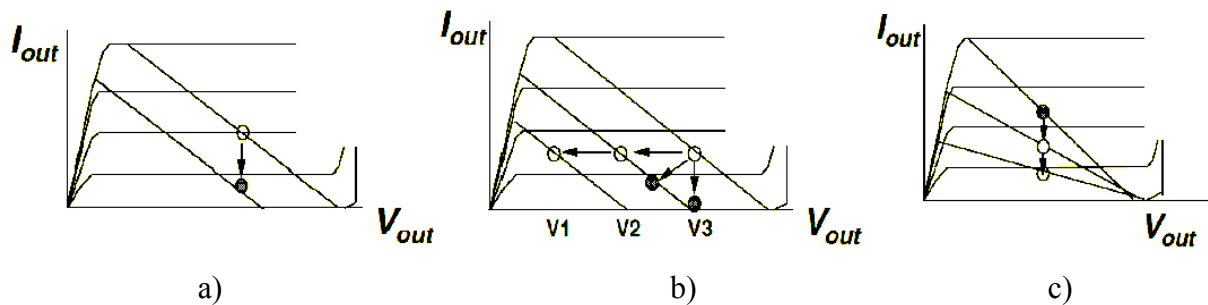


Figure 4.30 – Parameters to control the PA efficiency; a) polarization current, b) voltage supply VDD, c) load impedance

Following, the best known efficiency techniques are presented with appropriate references for further studies. At end of the section, the DPA design technique is presented and practical considerations are done on the next chapter.

4.9.1 Dynamic Polarization Technique

The Dynamic polarization technique consists in changing the transistor's gate polarization as the input signal power is changed with the objective to increase the PA efficiency or linearity. It is similar to the envelop tracking technique [8] [34] in which the PA drain DC polarization is controlled in according to the signal envelope [34].

The principle of the technique is presented in Figure 4.31 where a directional coupler samples the input signal and feeds an envelope detector. The detected signal is used to change the gate voltage due to change the DC current of the drain. The objective is to maintain the transistor always in a linear region without increasing to much the supply current on low input power levels.

Considering the ideal situation which the FET presents high input impedances, this control can be done with minimal energy consumption, thus, the efficiency increase by the technique is not lost on the feedback control circuit. The major problems on this technique are related to the linearity. Normally, a significant level of AM-AM distortion is caused due to the polarization change.

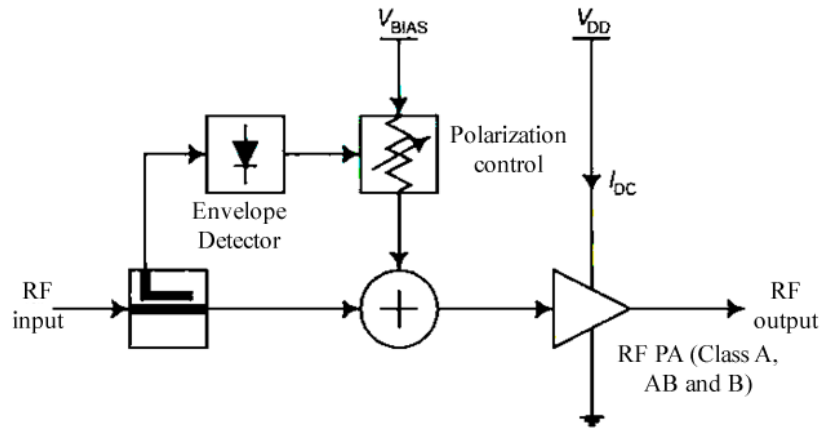


Figure 4.31 – Dynamic polarization technique diagram [34]

4.9.2 Envelope Elimination and Restoration Technique (EE&R)

The envelope elimination and restoration technique [8] [34] (Figure 4.32) consists in keeping the signal phase modulation by a limiter, which eliminates the possibility of phase distortion (AM-PM) on a non-linear PA. The signal amplitude envelope is restored at the output using a modulated supply voltage [1].

Actually, the envelope amplification process of the detected signal dissipates a considerable high level of power. Another problem is that the phase of the output signal changes with the input power, which causes distortion like the dynamic polarization technique.

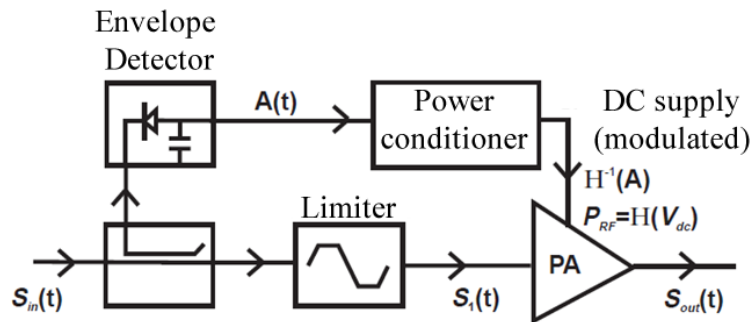


Figure 4.32 – Envelope elimination and restoration system [1].

4.9.3 Power Cell Switching Technique

The power cell switching technique [8] [45] [41] consists in building a PA with many amplifier cells in parallel that are switched in according to the input signal level. The Figure 4.33 presents a simplified diagram of this technique. This technique needs a control circuit to activate the switches on the PA's input and a network to combine the output power.

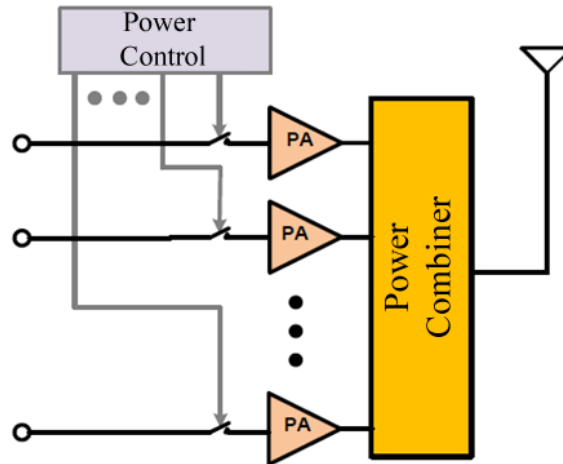


Figure 4.33 – Power cell switching techniques diagram [41].

This technique has the advantage to increase the output power and to reduce the linearity demands of each cell individually. The major problems are related to the chip area required, to the switching control circuit and to the losses produced by these switches during the PA operation.

4.9.4 Envelope Tracking Technique

The basic difference between the envelope tracking [8] [34] (ET) technique and the envelope elimination and restoration technique is that ET must use a PA class A, AB or B and not a non-linear PA (high efficiency class E or F).

The detector samples the envelope information from the modulated RF input signal and feeds an audio amplifier or a switching regulator. The objective is to provide to the RF PA only the needed supply for a linear amplification on the level of the instantaneous envelope on the sampling moment.

The supply control reduces considerably the energy consumption on low power levels, which increase the efficiency without compromising the linearity (on the ideal case) [34]. The simplified scheme of the technique is presented on Figure 4.34.

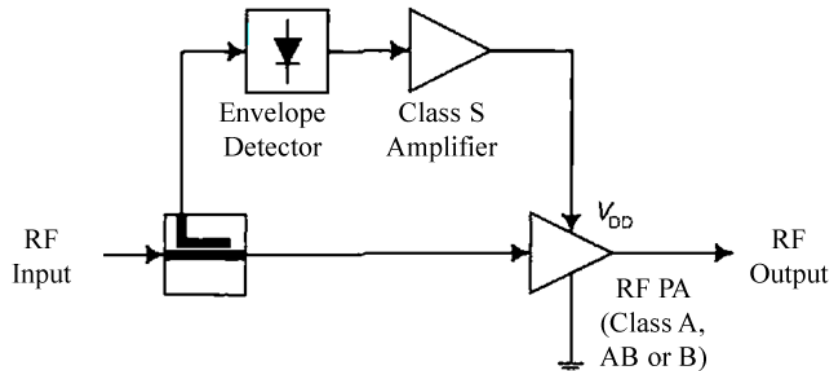


Figure 4.34 – Schematic of a RF PA using the ET technique [34].

4.9.5 Bypass Stage Technique

The by-pass stage technique [46] consists on changing the signal propagation path using parallel and series switching power cells for changing the load impedance. Each path is optimized for a different power level, with an optimal load.

The study [46] presents the application the bypass stage technique for creating a PA in which multiples operation modes with three different power stages can be chosen with a low DC polarization current. The PA structure (Figure 4.35) and its operation modes are presented in Figure 4.36.

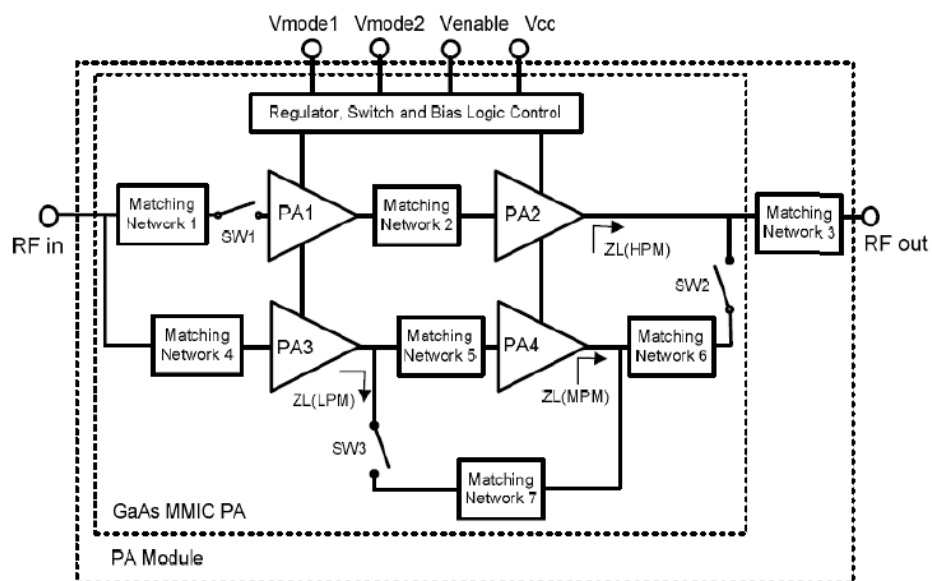


Figure 4.35 - Bypass stage technique structure

	Mode of Operation			
	Disable	HPM	MPM	LPM
PA1,2	OFF	ON	OFF	OFF
PA3	OFF	OFF	ON	ON
PA4	OFF	OFF	ON	OFF
SW1	OFF	ON	OFF	OFF
SW2	OFF	OFF	ON	ON
SW3	OFF	OFF	OFF	ON

Figure 4.36 – Bypass stage technique and its operation modes [46].

Challenges presented by this technique are the need of RF switches capable to support high power and to present reduced losses. Beyond that, there is a considerable gain variation between the operational modes which difficult a linear amplification when many stages must be turned on sequentially during the amplification of the same signal.

4.9.6 Doherty Technique

The Doherty Power Amplifier technique (DPA) (Figure 4.37) is the central theme of this thesis. It consists on a technique to increase the PA efficiency on the low/medium power region to present a constant efficiency performance from the backoff until the maximum output power [4] [1] [42] [34] [5]. Its basic principle consists on using the active load-pull effect in which an auxiliary PA changes dynamically the output impedance of a main PA to keep the PAE constant in a range of output power levels.

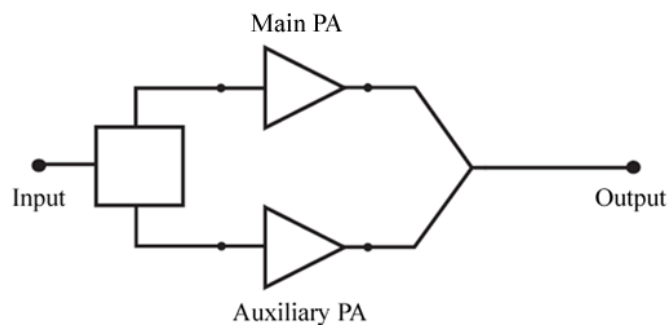


Figure 4.37 – Doherty power amplifier simplified schematic

The theoretical drain efficiency of the DPA is presented on Figure 4.38, in which the constant efficiency region is computed by the equation (9). This amplifier has two operation stages: a low power region and a high power region. Initially, only the main PA works (class B or AB) and the auxiliary PA remains off due to a class C polarization that need a high input signal to produce a current flow. As the input signal amplitude increases, the main PA reaches its saturation with the theoretical maximum efficiency of 78.5%. On this moment the signal have

enough amplitude to make the auxiliary PA to start to work. As the auxiliary PA current increases, the load seen by the main PA is decreased because of a quarter wave transmission line connected between the main PA and the load.

$$\eta = \frac{\pi}{2} \frac{\left(\frac{v_{in}}{V_{max}}\right)^2}{3\left(\frac{v_{in}}{V_{max}}\right) - 1} \quad (9)$$

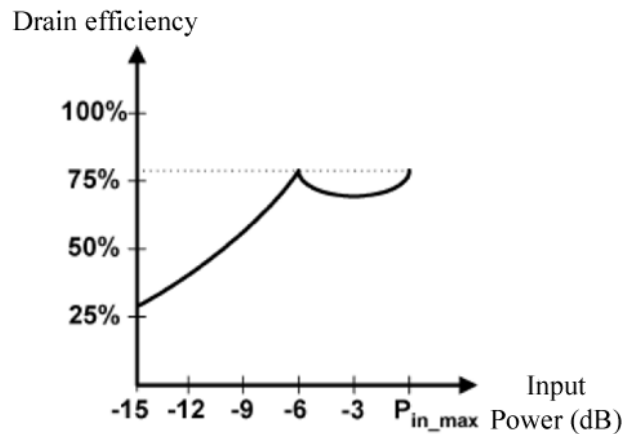


Figure 4.38 – Doherty power amplifier theoretical drain efficiency [1]

The DPA is on its high power region when the auxiliary PA works. In this region the efficiency and the drain voltage of the main PA are constant and the efficiency of the auxiliary PA increases until its maximum, on the maximum input signal amplitude. The constant efficiency region is designed to cover the PAPR value of the signal, solving the low PAE problem of the conventional PA on the backoff.

4.10 DOHERTY POWER AMPLIFIER THEORY

The DPA idea was created by W. H. Doherty in 1936 [21] as a technique to increase the efficiency on the backoff of linear PAs with valves. The idea is to provide high impedance on the first power stage to quickly saturate the PA and reach the maximum efficiency. Then, the impedance starts to be reduced by a second PA keeping the first PA saturated and with maximum efficiency. With electronics evolution, valves were replaced by transistors and the DPA technique had to be adapted.

The load modulation is done by the current control of an auxiliary PA after the main PA saturation. There are many ways to control auxiliary PA's current, as for example, transistors

size adjust, adaptive polarization, attenuators or DSPs [1]. The following section will present equations for a simplified DPA that controls the load modulation by a class C auxiliary PA.

4.10.1 Doherty Power Amplifier Load Modulation

Equations on this section are based on the DPA with main PA biased in class B and auxiliary PA in class C [47]. The load modulation effect is done in the DPA by a $\frac{1}{4}$ wave transmission line that is seen by the main PA (Figure 4.39). This line modulates the load and changes the main PA output signal phase in 90° , thus, this phase difference must be also made on the auxiliary PA signal, as shown in Figure 4.39 by the auxiliary PA voltage jv_G .

Main PA and auxiliary PA transistors must work as voltage controlled current sources (Figure 4.40). To demonstrate active load modulation effect, equations consider all parameters of Figure 4.39 as peak fundamental values. The parameters in Figure 4.39 are described in Table 4.3:

Table 4.3 – Description of the parameters from the circuit in Figure 4.39

Variable	Description
i_M	Main PA fundamental peak current
v_M	Main PA fundamental peak voltage
v_P	Auxiliary PA (or peak PA) fundamental peak voltage
i_P	Auxiliary PA fundamental peak current
v_G	Fundamental peak voltage in transistor's gate
i_L	Current peak on the load
R_L	Load resistance

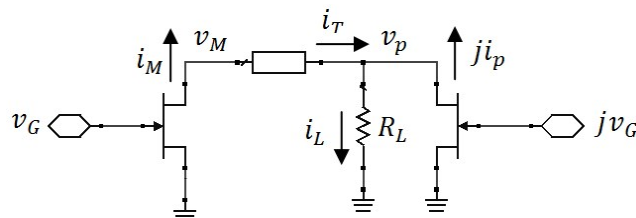


Figure 4.39 – Simplified scheme of Doherty power amplifier

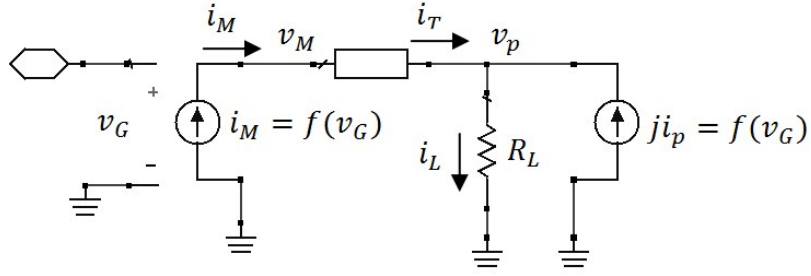


Figure 4.40– Transistors as voltage controlled current sources

The demonstration of the DPA equations starts by the parameters at the edges of the inversion transmission line (Figure 4.41) which have wave length of $L = 1/4$, angular frequency ω_0 and characteristic impedance Z_0 . Its transmission matrix is represented in equation (10):

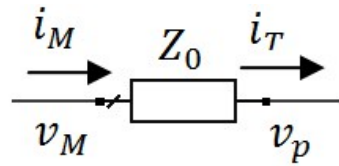


Figure 4.41 – Transmission line voltages and currents

$$T = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ j\frac{1}{Z_0} & 0 \end{bmatrix} \quad (10)$$

By equating parameters on transmission line edges and the matrix in (10), the voltage v_p on the load and the output current i_T from the transmission line can be computed:

$$\begin{bmatrix} v_p \\ i_T \end{bmatrix} = [T] \begin{bmatrix} v_M \\ i_M \end{bmatrix} \quad (11)$$

$$\begin{bmatrix} v_p \\ i_T \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ j\frac{1}{Z_0} & 0 \end{bmatrix} \begin{bmatrix} v_M \\ i_M \end{bmatrix} \quad (12)$$

Thus:

$$v_p = jZ_0 i_M \quad (13)$$

$$i_T = \frac{j}{Z_0} v_M \quad (14)$$

From equation (14), v_M can be computed:

$$i_T = \frac{j}{Z_0} v_M \quad (15)$$

$$v_M = \frac{i_T Z_0}{j} = -jZ_0 i_T \quad (16)$$

From the circuit in Figure 4.40, we get currents equations:

$$i_L = i_T + ji_p \quad (17)$$

$$i_T = i_L - ji_p \quad (18)$$

Replacing (18) in (16):

$$v_M = -jZ_0 i_T = -jZ_0 (i_L - ji_p) = -jZ_0 \left(\frac{v_p}{R_L} - ji_p \right) \quad (19)$$

$$v_M = -jZ_0 \left(\frac{jZ_0 i_M}{R_L} - ji_p \right) \quad (20)$$

$$v_M = \left(\frac{Z_0^2 i_M}{R_L} - Z_0 i_p \right) \quad (21)$$

The equation (13) and the Figure 4.40 demonstrate that the drain voltage v_p of the auxiliary PA depends only on the main PA drain current i_M and this current depends on the main PA gate voltage v_g . If the relation between the gate voltage and the drain current on the main PA is linear, the drain voltage on the auxiliary PA is also linear with the input signal.

The equation (21) describes main PA drain voltage. This equation is composed by two terms. The first term is related to the main PA current and to the load inversion. The second term is directly proportional to the auxiliary PA current. On the low power region, the auxiliary PA current is zero, thus, this equation will have only the first term. As the main PA current i_M increases, the voltage v_M also increases until reaching its maximum value. From the first term it is possible to verify that the main PA voltage increases quickly due to the square value on the impedance (Z_0^2). This factor saturates the transistor making it to reach its maximum efficiency.

When this saturation value is reached, the auxiliary PA must turn on making the second term on the equation to appear. As the auxiliary current depends also on the input signal, as the input power increases, the second term on the equation keeps the main voltage from increasing, not allowing the transistor to be damaged. This control occurs due to the 90° difference of phase on the signal from the auxiliary PA, thus, the design of this transmission line is essential.

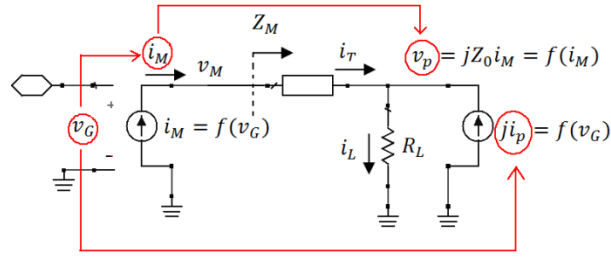


Figure 4.42 – Relations between the auxiliary transistors drain parameters and the voltage on the gate of the main transistor.

The active load modulation effect on the DPA can be observed by the equation of the main PA drain impedance (23).

$$Z_M = \frac{v_M}{i_M} = \frac{Z_0^2 i_M}{i_M R_L} - Z_0 \frac{i_p}{i_M} \quad (22)$$

$$Z_M = \frac{Z_0^2}{R_L} - Z_0 \frac{i_p}{i_M} \quad (23)$$

On the region that the auxiliary PA is not in operation, the impedance seen by the main PA is constant and equal to the first term of the equation (23). The increase of the auxiliary PA output current reduces the impedance seen by the main PA, as can be seen by the second term on the equation (23). The increase of the auxiliary PA output current also keeps constant the drain voltage of the main PA, which can be seen by equation (21). The two region of operation of the DPA can be seen in Figure 4.43.

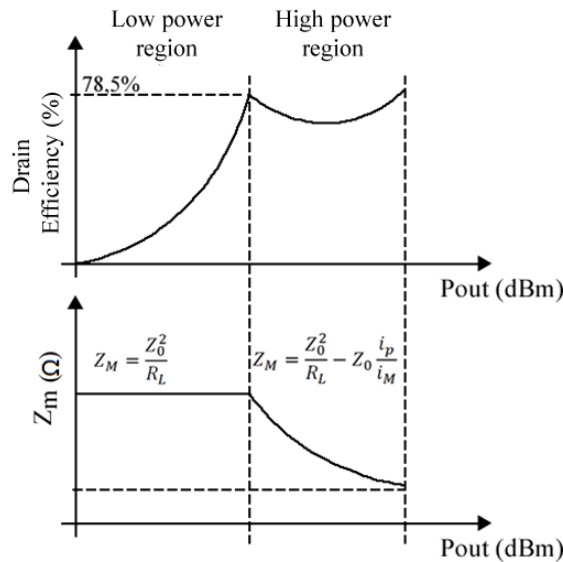


Figure 4.43 – Drain efficiency of the Doherty power amplifier and drain impedance of the main PA.

4.10.2 Sub-PAs Output Currents Equations

The ideal and classic DPA has sub-PAs with currents behavior as presented in Figure 4.44. To demonstrate sub-PAs operation, the ideal circuit presented on Figure 4.45 will be used. This simplified schematic uses ideal transistors with behavioral model represented on Figure 4.46. Parameters of the circuit in Figure 4.45 are described in Table 4.4.

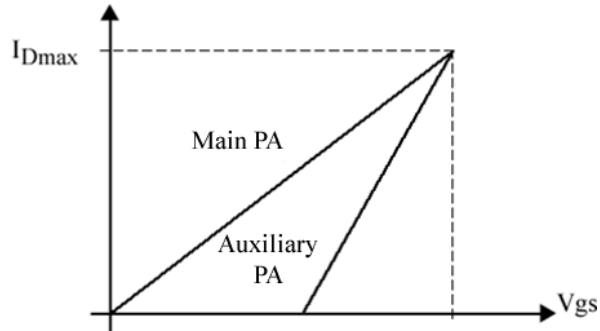


Figure 4.44 – Sub-PAs currents behavior

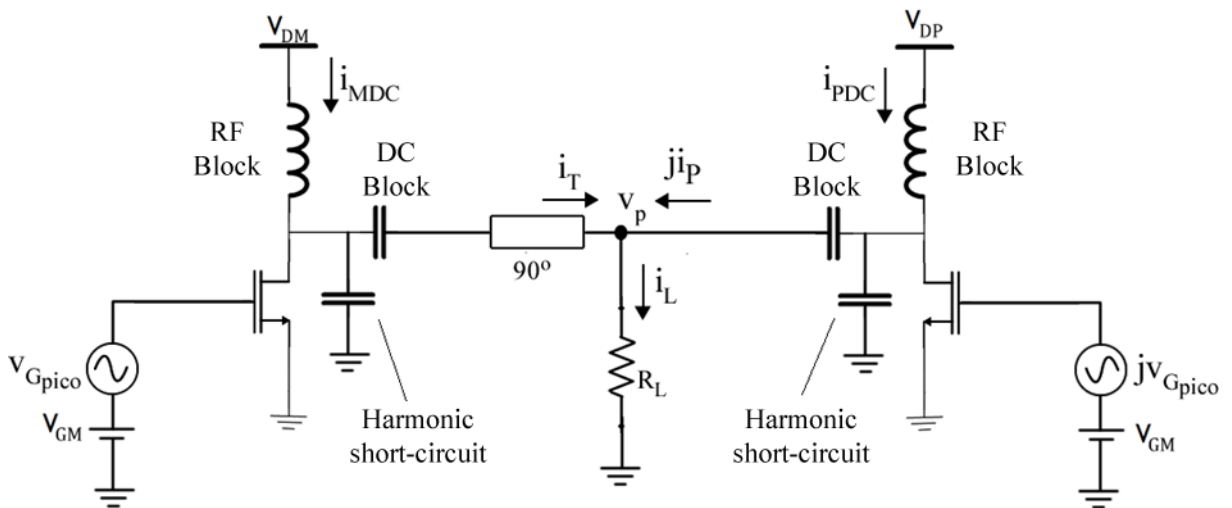


Figure 4.45 – Doherty power amplifier ideal circuit [47]

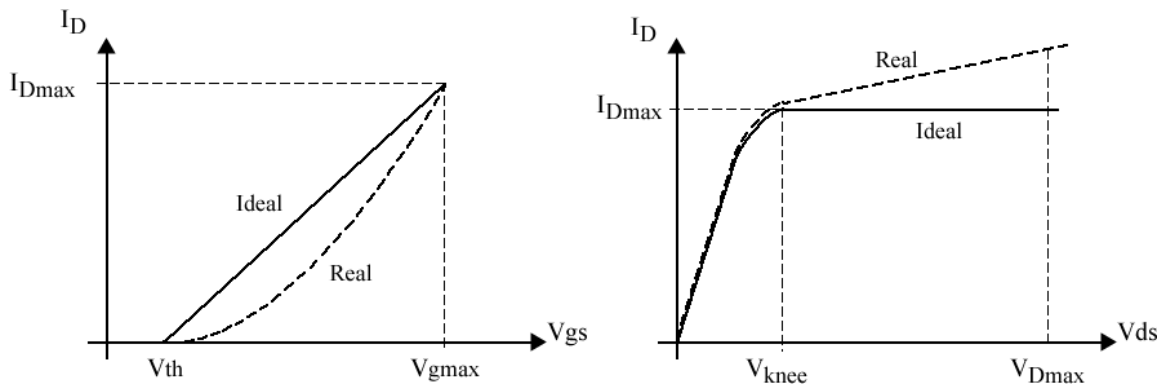


Figure 4.46 – Real and ideal transistor's model

Table 4.4 – Parameters of the simplified DPA of the Figure 4.46

Variable	Description
V_{gmax}	Gate maximum voltage
V_{dmax}	Drain maximum voltage
I_{Dmax}	Drain maximum current
V_{th}	Transistor threshold voltage
V_{knee}	Transition voltage between triode and saturation region

The large signal transfer function for the current of the simplified transistor is defined in equation (24):

$$i_D = \begin{cases} 0 & , V_g \leq V_{th} \\ I_{Dmax} \cdot \frac{v_g - V_{th}}{V_{gmax} - V_{th}} & , V_g < V_{th} \leq V_{gmax} \end{cases} \quad (24)$$

The polarization on the transistor's gate defines the operational class of the PA. In a class B PA the conduction angle α is of 180° . The conduction angle of the class C PA depends on the gate voltage and the input signal amplitude. Using the transistor's gate voltage equation and the Figure 4.47, the equation of the conduction angle α will be demonstrated as following:

$$v_G(t) = V_G + V_{Gpeak} \cdot \cos(\omega_0 t) \quad (25)$$

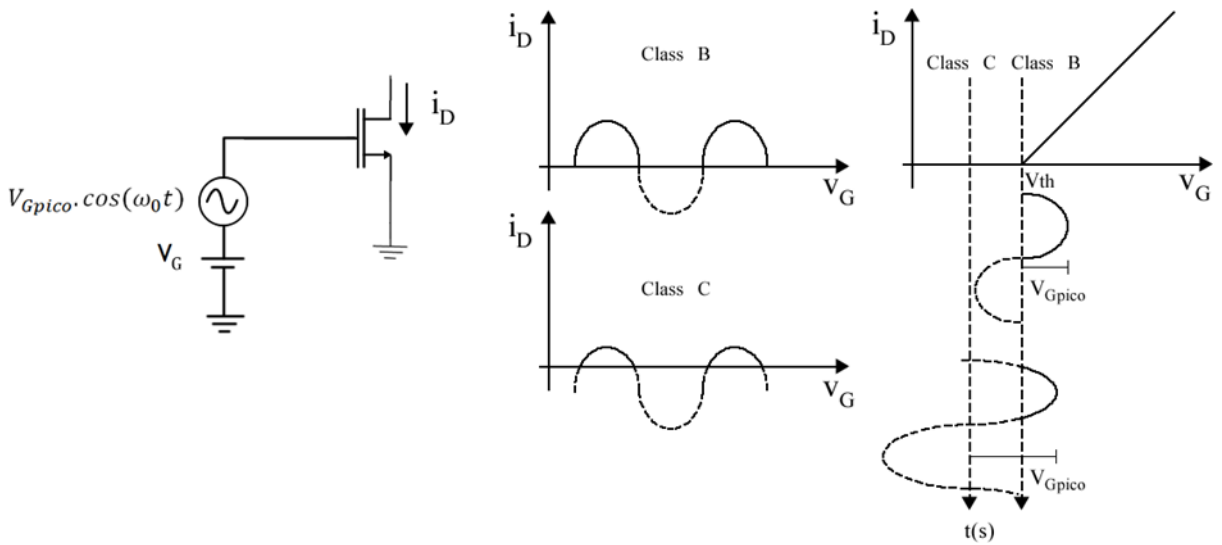


Figure 4.47 – Transistor gate voltage and sub-PA classes

Replacing (25) in (24), the time equation of the transistor drain is obtained:

$$i_D = \begin{cases} 0 & , V_g \leq V_{th} \\ I_{Dmax} \cdot \frac{V_G + V_{Gpeak} \cdot \cos(\omega_0 t) - V_{th}}{V_{gmax} - V_{th}} & , V_g < V_{th} \leq V_{gmax} \quad e \quad -\frac{\alpha}{2} \leq \omega_0 t \leq \frac{\alpha}{2} \end{cases} \quad (26)$$

The drain current is defined in the period $-\pi \leq \omega_0 t \leq \pi$ as:

$$i_D = I_{Dmax} \cdot \frac{V_G - V_{th}}{V_{gmax} - V_{th}} + I_{Dmax} \cdot \frac{V_{Gpeak} \cdot \cos(\omega_0 t)}{V_{gmax} - V_{th}} \quad (27)$$

$$i_D = I_Q + i_d \quad (28)$$

Thus:

$$I_Q = I_{Dmax} \cdot \frac{V_G - V_{th}}{V_{gmax} - V_{th}} \quad (29)$$

$$i_d = I_{Dmax} \cdot \frac{V_{Gpeak} \cdot \cos(\omega_0 t)}{V_{gmax} - V_{th}} = i_{Dpeak} \cdot \cos(\omega_0 t) \quad (30)$$

and :

$$i_{Dpeak} = \frac{I_{Dmax} \cdot V_{Gpeak}}{V_{gmax} - V_{th}} \quad (31)$$

Using Figure 4.48, the transistor conduction angle equation can be defined as:

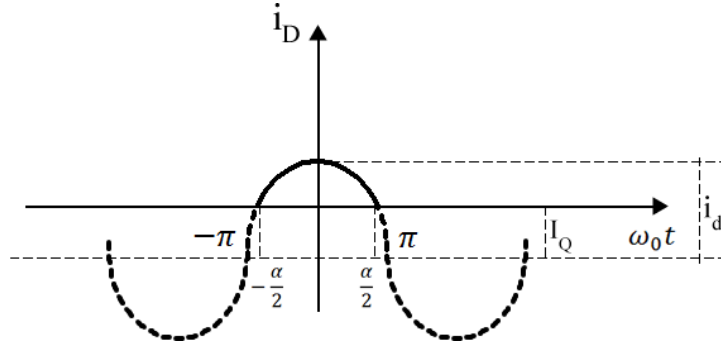


Figure 4.48 – Transistor conduction angle

If $\omega_0 t = \frac{\alpha}{2}$ thus $i_D = 0$, then:

$$i_D = I_{Dmax} \cdot \frac{V_G - V_{th}}{V_{gmax} - V_{th}} + I_{Dmax} \cdot \frac{V_{Gpeak} \cdot \cos(\omega_0 t)}{V_{gmax} - V_{th}} \quad (32)$$

$$0 = V_G - V_{th} + V_{Gpeak} \cdot \cos\left(\frac{\alpha}{2}\right) \quad (33)$$

$$\alpha = 2 \cdot \cos^{-1}\left(\frac{V_{th} - V_G}{V_{Gpeak}}\right) \quad (34)$$

The conduction angle is used on the currents and power calculations. For making the equation of the DC and fundamental component of the currents of each sub-PA the Fourier decomposition must be applied on the equation (26). The result for the class C PA is presented in (35) for the DC component and in (36) for the fundamental component.

$$i_{Dp_DC} = a_0 = \frac{1}{2\pi} \frac{I_{Dmax}}{V_{gmax} - V_t} V_{Gpeak} \left[2 \sin\left(\frac{\alpha}{2}\right) - \alpha \cos\left(\frac{\alpha}{2}\right) \right] \quad (35)$$

$$i_{Dp_ω0} = a_1 = \frac{1}{2\pi} \frac{I_{Dmax}}{V_{gmax} - V_t} V_{Gpeak} [\alpha - \sin(\alpha)] \quad (36)$$

The DC current component of the class B PA is represented by (37) and its fundamental component is represented by (38).

$$i_{Dp_DC} = a_0 = \frac{1}{\pi} \frac{I_{Dmax}}{V_{gmax} - V_t} V_{Gpeak} \quad (37)$$

$$i_{Dp_ω0} = a_1 = \frac{1}{2} \frac{I_{Dmax}}{V_{gmax} - V_t} V_{Gpeak} \quad (38)$$

4.10.3 Design Equations and Doherty Power Amplifier Performance

The DPA currents behavior and the active load-pull effect are the main factors that define a DPA efficiency constant length performance. The DPA efficiency backoff length is defined by the moment that the auxiliary PA starts to operate, which starts the main PA load reduction and makes constant the main PA drain voltage. Thus, if the auxiliary PA starts to conduct before the main PA gets into its maximum efficiency (saturation), the DPA efficiency will be limited on the level that it was when the auxiliary PA started to operate.

The auxiliary PA starts its conduction in a level defined by V_{bk} (break point voltage) (39). The “k” factor is defined as the percentage of the maximum peak voltage on the gate of the main transistor that corresponds to level which the auxiliary PA starts to conduct. The classic DPA has always a k of 0.5, which creates a drain efficiency curve with constant performance in 6dB backoff. This factor is one of the parameters that can increase the backoff length of the DPA, creating the asymmetric DPA [47] [48].

$$V_{bk} = k(V_{gmax} - V_{GM}) = k(V_{gmax} - V_{th}) \quad (39)$$

When the “k” factor is above 0.5, the auxiliary PA starts to conduct early and its maximum output current must reach a higher level in relation the main PA maximum output current for the DPA to present a PAE performance with both peaks on the same level. In relation to the

level of the output current of the main PA and the auxiliary PA on the maximum output power the DPA can receive different classifications [1]:

- Classic or symmetric DPA:** output current of both sub-PAs reach the same maximum level.
- Asymmetric DPA:** output current of the auxiliary PA surpasses the current of the main PA.
- DPA lite:** output current of the auxiliary PA reaches a lower level in relation to the main PA maximum current [1].

In [47] the remaining design equations of the DPA are demonstrated and defined as presented in Table 4.5. In this table, V_{GM} represents the main PA gate polarization, V_{GP} represents the auxiliary PA gate polarization, V_D the drain voltage of both sub-PAs, I_{Pmax} the maximum current of the auxiliary PA, I_{Mmax} the maximum current of the main PA, Γ is the ratio between auxiliary PA and main PA output currents.

Table 4.5 – Design Equations of the Doherty Power Amplifier

Equation	Ref.
$V_{GM} = V_{th}$	(40)
$V_{GP} = (k + 1)V_{th} - kV_{Gmax}$	(41)
$V_D = \frac{V_{Dmax} + V_{knee}}{2}$	(42)
$I_{Mmax} = \frac{8kP_{Lmax}}{V_{Dmax} - V_{knee}}$	(43)
$I_{Pmax} = \Gamma I_{Mmax}$	(44)
$\Gamma = \pi \frac{1/k - 1}{\alpha_{Pmax} - \sin(\alpha_{Pmax})}$	(45)
$\alpha_{Pmax} = 2 \cos^{-1}(k)$	(46)

In Table 4.6 the equations for the maximum output power on the load (P_{Lmax}), the DC power supply and drain efficiency are presented for the low power region. Table 4.7 presents the same measures for the high power region.

Table 4.6 – Load power, DC power and drain efficiency on the low power region

Equation	Ref.
$P_L = \frac{1}{2} \Re\{v_M i_{M\omega 0}^*\} = \frac{Z_0 I_{Mmax}^2}{8k(V_{Gmax} - V_{th})} v_{Gpico}^2$	(47)
$P_{DC} = V_D i_{MDC} = \frac{I_{Mmax}(V_{Dmax} + V_{knee})}{2\pi(V_{Gmax} - V_{th})} v_{Gpico}$	(48)
$\eta_D = \frac{P_L}{P_{DC}} = \frac{\pi Z_0 I_{Mmax}}{4k(V_{Dmax} + V_{knee})(V_{Gmax} - V_{th})} v_{Gpico}$	(49)

Table 4.7 – Load power, DC power and drain efficiency on the high power region

Equation	Ref.
$P_L = \frac{1}{2} \Re\{v_P i_L^*\} = \frac{1}{2} \Re\left\{\frac{ v_P ^2}{R_L}\right\} = \frac{Z_0 I_{Mmax}^2}{8k(V_{Gmax} - V_{th})} v_{Gpico}^2$	(50)
$P_{DC} = V_D i_{MDC} + V_D i_{PDC}$	(51)
$P_{DC} = \frac{I_{Mmax}(V_{Dmax} + V_{knee})}{2\pi(V_{Gmax} - V_{th})} v_{Gpico} \left\{1 + \frac{\Gamma}{2} \left[2 \sin\left(\frac{\alpha_P}{2}\right) - \alpha_P \cos\left(\frac{\alpha_P}{2}\right)\right]\right\}$	(52)
$\eta_D = \frac{\pi Z_0 I_{Mmax}}{4k(V_{Dmax} + V_{knee})(V_{Gmax} - V_{th})} \frac{v_{Gpico}}{1 + \frac{\Gamma}{2} \left[2 \sin\left(\frac{\alpha_P}{2}\right) - \alpha_P \cos\left(\frac{\alpha_P}{2}\right)\right]}$	(53)

The Figure 4.49 presents the drain efficiency performances of a symmetric DPA (6dB backoff) and an asymmetric DPA (10dB backoff) plotted with presented equations (on the left) and the currents of the sub-PAs for the symmetric DPA (in the middle) and for the asymmetric DPA (on the right). It can be observed that the extension on the efficiency performance is due to the moment which the auxiliary PA starts to conduct and due to its maximum output current level.

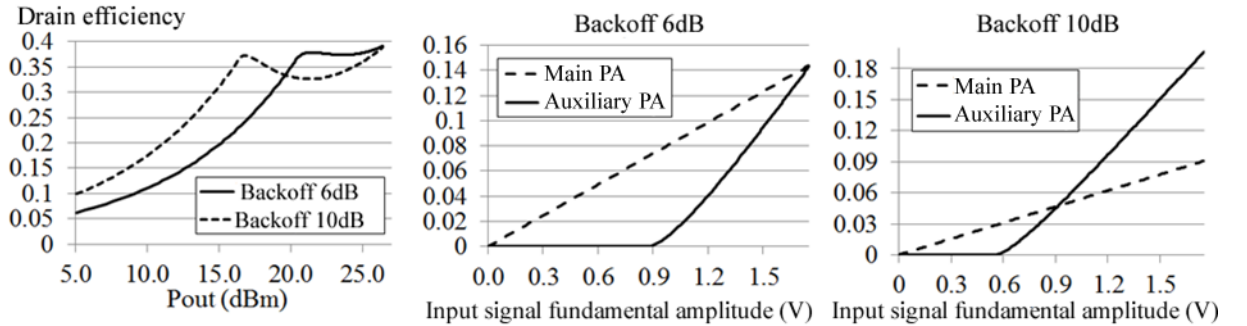


Figure 4.49 – Relation between the constant efficiency and the sub-PAs currents behavior

Another factor of great importance on the DPA performance is the value of the V_{knee} voltage. The impact of this voltage on the DPA maximum efficiency level is demonstrated in Figure 4.50.

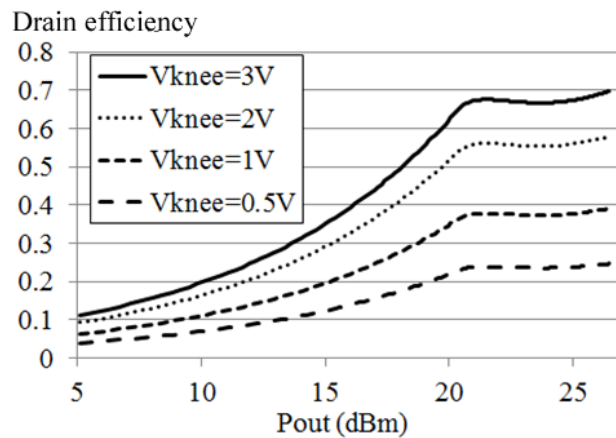


Figure 4.50 – Impact of the V_{knee} voltage on the DPA efficiency

DPA design equations are important for showing the circuit operation and for giving an insight of the role of each parameter on the performance. However, due to imperfections on real components (parasites) and non-linearity, it can't be expected a good approximation between these simple equations and simulation results. The DPA design is based on an iteration cycle that will be discussed on the following sections.

4.11 DOHERTY POWER AMPLIFIER STATE OF THE ART

The active load modulation that happens in the DPA can be done in different ways. This flexibility made possible the creation of many types of DPA:

DPA Lite: transistors of the main PA (class AB/B) and the auxiliary PA (class C) have the same dimensions, thus, the maximum current of the auxiliary PA does not reach the same level of the main PA current due to the different polarization, producing a DPA with only a slightly increase of efficiency in the backoff [1].

Asymmetric DPA: the main PA (class AB/B) and the auxiliary PA (class C) have different dimension and normally the maximum output current of the auxiliary PA surpasses the maximum current of the main PA [49].

DPA combined with the envelope tracking technique: consists on the use of two efficiency enhancement techniques on the same time in the PA [50].

Interleaved DPA: consists on a DPA with multiple stages composed by multiples auxiliary and main PAs that are connected alternately which interleaves many auxiliary and main PAs together [51].

DPA with a filter in the auxiliary PA: consists on a DPA with both sub-PAs with the same size and polarization. The increase on the auxiliary PA current is done by a controlled filter that is connected to its input [34].

Inverted DPA: consists on a DPA where the inverter transmission line is connected to the auxiliary PA drain instead of the main PA drain [52].

DPA with auxiliary PA in class E: class E PAs has similar non-linearity to the class C PAs but higher PAE performance which is favorable for increasing the whole PAE of the DPA [53].

DPA with auxiliary PA in class F: consists on the use of a class F instead of a class C on the auxiliary PA to increase the maximum efficiency of the DPA [54].

DPA with adaptive polarization: consists in controlling the auxiliary PA current by changing dynamically its polarization. On the low power region, the auxiliary PA must have a class C polarization and as the input signal increases, this polarization is gradually changed towards the class B. Another possibility of this kind of DPA is the control of the drain voltage of the auxiliary PA [48].

DPA with multiple stages: consists on a DPA with many auxiliary PAs and one main PA. This DPA produce a PAE performance with many peaks and a higher extension toward the backoff. Successful implementations have already been done in PCB, however, an integrated DPA with multiple stages require a great area due to its large network matching, which produces considerable losses [55].

Many DPAs have been already implemented in PCB, normally for radio base stations (BTS). Integrated implementations have also been done in many technologies as InGaP, GaAs, GaN, HEMT and CMOS (180nm, 130nm, 90nm, 65nm). In on-chip implementations, normally, part of the circuit is integrated (transistors) and other part goes to the PCB (normally the network matching and choke inductances). In the case of the 65nm CMOS technology there are only few published conventional PAs and for the knowledge of the authors, only one DPA published [3]. This last reference presents a circuit with the DPA structure but its performance does not present the constant PAE curve that is the main characteristic of the DPA.

The Table 4.8 presents a synthesis of many DPAs with AB/C topology published on last years and that were consulted during this research. It can be observed that even for expensive and high performance technologies the PAE performance level of the DPA is around 40% and the PAE with the constant behavior is found in PCB or partially integration implementations. Fully DPA integration presents only a slightly increase in PAE on the backoff in relation the conventional PAs class AB/B. DPAs with higher PAE performances [56] [57] in practice do not present any increase of PAE on the backoff, thus, they correspond to PAs with the Doherty structure but without its main functional characteristic.

Table 4.8 – Previous work on the Doherty Power Amplifier

Ref.	Year	Freq. (GHz)	Technology	Pout (dBm)	Gain (dB)	PAE (%) Max.	PAE(%)		Topology
							@0dB/3dB	/7dB/10dB	
[75]	1999	17	GaAs HEMT	25	8	39	39/37/27/15	AB/C	
[58]	2000	20	GaAs HEMT	23	18	37	37/26/18/13	AB/C	
[59]	2003	2.4	CMOS 0.25um	25	10	43	37/41/34/25	AB/C	
[62]	2006	1.7	0.13um CMOS	31.5	40	36	36/31/22/19	AB/C	
[57]	2006	2.4	0.13um CMOS	23	25	65	65/60/45/30	AB/C	
[11]	2006	3.65	90nm CMOS	26.5	26	35	35/27/10/5	AB/C	
[61]	2007	0.8	InGaP/GaAs HBT	28	27	43	43/40/36/30	Dynamic polarization	
[64]	2007	5	90nm CMOS	25	24	21	21/20/13/6	AB/C	
[65]	2007	38-46	GaAs HEMT	21.8	9	25	25/20/22/15	AB/C with Pre-distortion	
[59]	2008	2.4	0.18um CMOS	21.5	12	15	15/12/10/6	AB/C cascode- cascade	
[75]	2008	60	0.13um CMOS	7.8	13	3	3/2/1/0	AB/C	
[60]	2009	2.4	0.18um CMOS	22.4	20	44	44/41/37/29	AB/C	
[12]	2010	2.4	90nm CMOS	20.5	16	27	27/21/12/7	AB/C	
[13]	2011	2.4	90nm CMOS	26	18	33	33/30/26/18	AB/C	
[56]	2011	2.4	GaN	44	13	70	70/60/52/43	Dynamic polarization	
[3]	2012	2.4	65nm CMOS	30.5	27	34	34/30/20/15	AB/C	

The most part of integrated DPAs implements the basic AB/C topology. Variations on component values in the fabrication, the impact of parasites and high costs of chip area make implementations of multi-stage DPAs and DPAs with class E or F auxiliary PAs to be very expensive due to the area required by the great number of inductors. Another drawback of using many inductors are losses due to the low quality factor on CMOS technology. Class E PAs present PAE levels higher than the class C, however, they present similar challenges on increasing the output power. Class E PAs are also highly tuned which make variations on the components to produce a considerable impact on the measured performance.

Works [58], [57], [59], [60], [16], [17], [3] present DPAs with frequencies near to this research, 2.535 GHz, and the CMOS technology. Works [16], [17] were done in 90nm

CMOS, which present characteristics more similar to the 65nm in relation to the others publications.

The work [17] is one of the most recent publications with nearer characteristics. Transformers were used to realize the multiple function of power splitter and inverter transmission line with the objective to solve the low quality factor presented by lumped transmission lines.

The work [61] presents a DPA with adaptive polarization for low frequencies. Due to the low frequency, it uses lumped components on the circuit which provided important details for designing the power splitter, the inverter transmission line and the network matching. Other works that provided important information for designing a DPA in 2.535 GHz were [62], [56], [59].

4.12 CONCLUSIONS

In this chapter, equations for performance parameters in PAs, classes of operation, power cells topologies, the load-pull/source-pull technique, the conventional design methodology for integrated PAs and many efficiency enhancement techniques were presented. Among the enhancement efficiency techniques, the DPA corresponds to the main study on this thesis. The DPA equations and its bibliographic review were presented. It can be concluded that most part of DPAs successful implementations are for PCBs and that there are yet many challenges for a fully integration implementation.

5 DOHERTY POWER AMPLIFIER DESIGN METHODOLOGY, CIRCUIT DESCRIPTION AND SIMULATIONS

5.1 INTRODUCTION

This chapter presents the iterative conventional PA design methodology going from the schematic until the final layout for fabrication. Following, an analysis of the problems in this methodology is done when it is applied on the DPA design and then a new methodology based in sequential optimizations is proposed. This chapter presents the designed layout with details of all its components and simulations. Finally, one last optimization methodology based on the electromagnetic modeling of layout paths is proposed with the objective to mitigate parasites effects.

5.2 CONVENTIONAL DOHERTY POWER AMPLIFIER DESIGN METHODOLOGY ANALYSIS

As presented in the last section, the conventional design methodology for PAs goes through for many design loops. The main problem related to this methodology is the great number of operations that must be done to reach a good performance, which also requires much time and effort from the designer. The analysis of this design process for the cascode and differential topologies shows with even more emphasis this problem.

It can be observed in Figure 5.1 four iteration loops, one inside the other, for the cascode PA design. The differential topology design follows an analog process with the critical detail that after the determination of the optimal input/output impedance, two new baluns must be designed. The balun design is a complex task [63] which can be aided by dedicated software that reduces the design time from many days to a couple of hours.

Due to these problems, PAs design is a long process. When there is not enough time to realize all this manual optimization process, the PA is normally designed with over-dimensioned values due to produce the required output power with great losses due to mismatch, which reduces considerable the PAE performance.

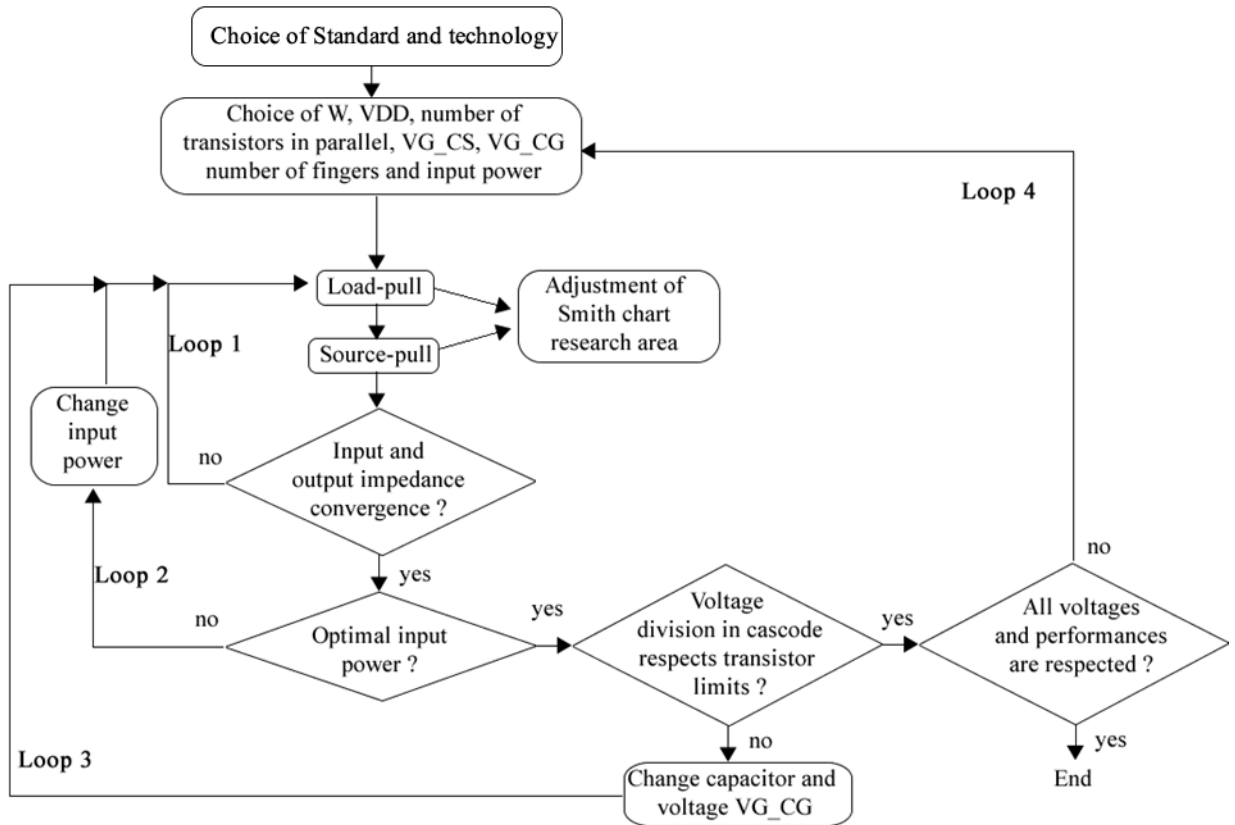


Figure 5.1 – Cascode PA design flowchart

Due to the time and effort required, this conventional PA design methodology is not practicable for designing a DPA. The DPA is composed by two PAs, at least, that must work in a synchronized way, beyond presenting a complex network matching to realize the active load-pull effect on the main PA load and to correctly offset the current phase of the auxiliary PA.

At the end of the design of the main and auxiliary PA, their behaviors must be overlapped in the same graph for analyzing if they are capable to work together and reach the specifications of the DPA. Normally, the designer finds that the first group of designed sub-PAs is not satisfactory, requiring changes in each one of them and re-starting a long cycle of iterations. After many attempts of designing a DPA with this conventional methodology, it was realized that it is not a feasible way due to the long time and effort required. These problems conducted to the development of a new design methodology that is presented on the next section.

5.3 STUDY ON THE DOHERTY POWER AMPLIFIER TOPOLOGY AND SUB AMPLIFIERS CLASSES

The different classes of auxiliary PA and the possibility to add a driver in the DPA structure generates many possible topologies. The Table 5.1 presents five different topologies of DPA, the expected number of inductors and the main advantages and disadvantages.

The main challenge/problem on designing a fully integrated DPA is on the number of inductors required. The Table 5.1 predicts the number of required inductors considering sub-PAs with the common-source or cascode topology with each one using a choke inductance. On the circuits with a driver, it is considered that the driver's choke is enough to make the inter-matching with the PA, thus, only one inductor is considered for the driver's choke and inter-matching. Each transmission line requires one inductor and the power splitter requires two inductors. When the power splitter is connected directly to the source it is not considered an input matching at this point, however, when there is a driver directly connected to the source an input matching is considered in this point, so an inductor is needed.

All topologies presented in Table 5.1 have a number of inductors considered excessive to be integrated on the chip. Due to the required area and the low quality factor of integrated inductors, the number of this type of component is the most critical factor on the fully integrated DPAs. Inductors increase losses, reduces the performance, increases the chance to produce undesirable mutual inductive effects and increases the chip cost (chip area).

The Table 5.1 indicates the main challenges on the DPA implementation due to the auxiliary PA class and the existence or not of a driver. When a driver is used together with a class C, the gain problem is solved but the low efficiency problem is added. The topology 1 presents the lowest number of inductors; however, 10 inductors are yet an excessive quantity to be integrated. The following sections will show that the topology 1 was chosen to be implemented and that an optimization technique applied on the input and output networks was capable to reduce the number of inductors to eight.

Table 5.1 – DPA Topologies

Ref.	Topology	N° Ind.	Challenges/ Problems	Advantages
Top. 1		10	Low gain on the class C	Simplicity
Top. 2		11	Low efficiency on the auxiliary PA branch	Gain increase on the auxiliary PA
Top. 3		12	Low overall efficiency on the DPA	Correction on the gain of the auxiliary PA by an uneven power splitter
Top. 4		13	- High complexity of the class F and E PA. - Low output power and gain on the auxiliary PA branch. - High non-linearity	High efficiency level (theory)
Top. 5		12	- High complexity of the class E PA. - Low output power and gain on the auxiliary PA branch. - Low performance of the class C as a driver. - High non-linearity	High efficiency level (theory)

Beyond the increase of cost and reduction of performance caused by the number of inductors, there are constructive restrictions on the 65nm CMOS technology that limits the number of inductors inside a chip. To fabricate the chip, many rules related to the density of metal in each layer must be respected.

It can be observed in Table 5.1 that switching PA classes can be used due to increase the efficiency level of the DPA. Due to the budget limit of 3 mm², the chronogram of the project and the density restrictions, all topologies that required more inductors and area were discarded.

5.4 NEW DESIGN METHODOLOGY PROPOSAL FOR THE DOHERTY POWER AMPLIFIER

The developed design technique considers the DPA theory, the challenges of the 65nm CMOS technology and the design environment of ADS. Due to the great number of restrictions to be respected and the great number of parameters to be sized (33 restrictions and 48 parameters in the final circuit), it is necessary to setup different optimization schematics in ADS. It was developed one specific optimization schematic for each sub-PA and a result analysis environment to show the performance of both sub-PAs in the same time and with overlapped curves during the optimization. It was also developed a test schematic to connect the sub-PAs in the DPA structure.

The Figure 5.2 presents a simplified diagram that explains the design sequence of the DPA in according to the proposed methodology. In the next sections, each design step will be presented in details.

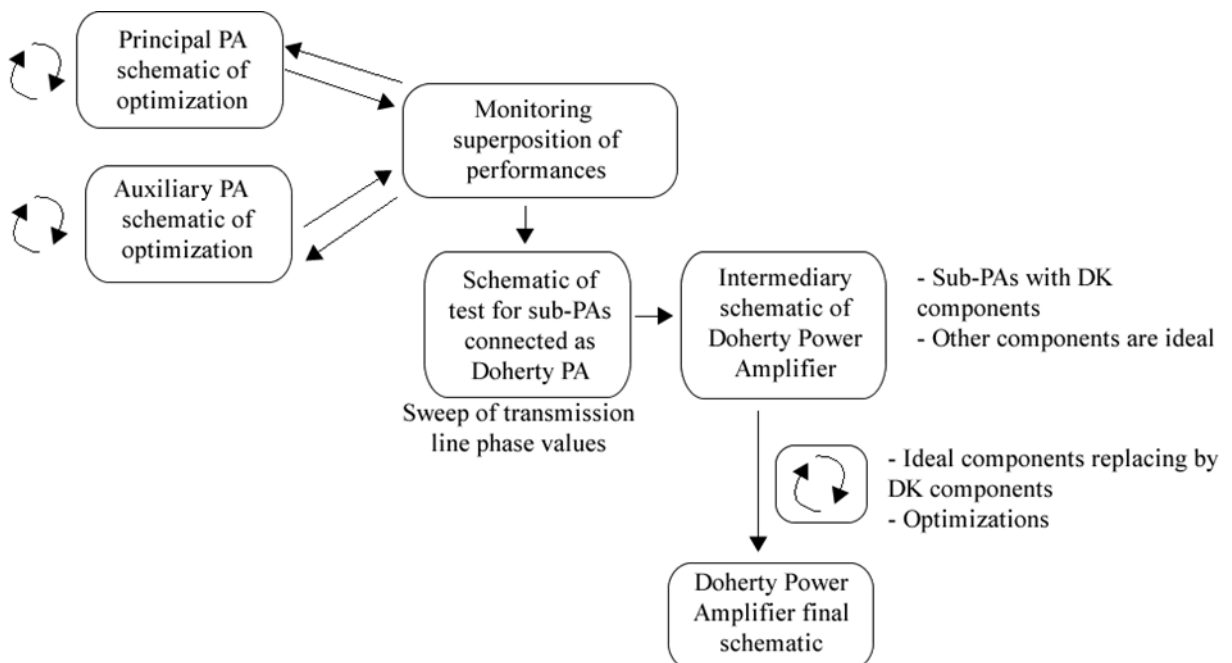


Figure 5.2 – Simplified diagram of the design cycle of the Doherty Power Amplifier

5.4.1 Impedance Analysis on the Doherty Power Amplifier

Before starting the sub-PAs design it is important to observe the impedance of the main branches in the DPA when it works on the maximum output power. It can be observed in Figure 5.3 that due to the source impedance of 50Ω , the Wilkinson power splitter presents also 50Ω in each output. On the main PA input, it must be designed a network matching between 50Ω and the optimum impedance of this PA. In the auxiliary PA branch, it must be added a dephasing transmission line of 90° ($\lambda/4$ wavelength) with characteristic impedance Z_0 of 50Ω and match this impedance with the optimum input impedance of the auxiliary PA.

The output matching network of the DPA is composed by a network that adapts the main PA optimum output impedance with the inverter transmission line (90° or $\lambda/4$ wavelength and Z_0 of 100Ω). The auxiliary PA output matching is also done to 100Ω for presenting an equivalent impedance of 50Ω and finally match with the final load of 50Ω .

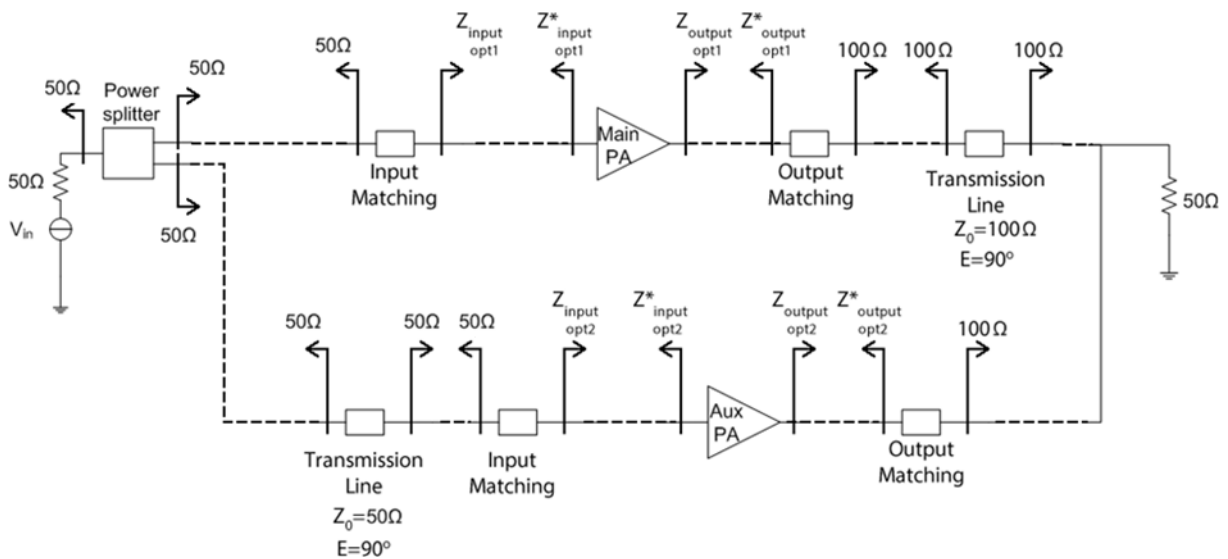


Figure 5.3 – Doherty Power Amplifier impedance analysis

According to the diagram in Figure 5.3, the main and auxiliary PAs are designed to an input impedance of 50Ω and an output impedance of 100Ω [64] [65] [15]. After designing the sub-PAs, the next step is to design the power splitter, the inverter and dephasing transmission line.

It is considered more appropriate to start the DPA design by the auxiliary PA because it must present the greater output power and its restrictions defines the most important limitations on

the DPA. As the auxiliary PA is biased in class C, it is harder to increase its output power than a class AB. The compression point of the auxiliary PA also defines the maximum output power and compression point of the main PA, which will result on the length of constant efficiency of the DPA. Anyway, after the first version of sub-PAs, some iteration is needed to adjust their performances until reaching the desired DPA.

5.4.2 Sub-PAs Design

The cascode topology was chosen for each sub-PA due to its capacity of supporting a high supply voltage VDD and the chip area limitation. Tests on the common-source topology presented a maximum output power far from the required level and the differential topology was not suitable for the project due to chip area limitations (3mm^2), the available time and foundry fabrications dates.

The design schematics for the main and auxiliary PA were done with the same topology, being different only by the variables index and values. Variables from the main PA received the suffix “_PA1” and from auxiliary PA the suffix “_PA2”.

The conventional load-pull and source-pull methods represent with four values (a_1 , a_2 , b_1 and b_2) the input and output optimum impedances of the PA, which correspond to $Z_{in}=(a_1+j*b_1)$ and $Z_{out}=(a_2+j*b_2)$. After defining this impedances, the next step is to design two L network matching that will be composed by two capacitors (C1 and C2) and two inductors (L1 and L2). The gradient optimization process replaces the load-pull/source-pull cycle and the network matching design by a direct search on the four values L1, L2, C1 and C2.

The complete schematic of the sub-PAs is shown in Figure 5.4. Assigning fixed values for polarization and transistor's size, the gradient optimization process does not present the local minimal problem when searching for the ideal input and output matching in the PA when the L-network matching type is used (four search variables). When the size of the transistors, the gate polarization of the common gate transistor (CG) and the capacitor C3 (Figure 5.4) are added to the optimization search process, it continues to present a good convergence without being affected by local minimal problem. However, if the drain voltage VDD and the voltage on the gate of the common source transistor (CS) are added on the gradient optimization process, the search space starts to present minimum local points due to the non-linear

behavior of the transistor. Thus, it can be observed that the algorithm converges to different performances depending on the initial conditions.

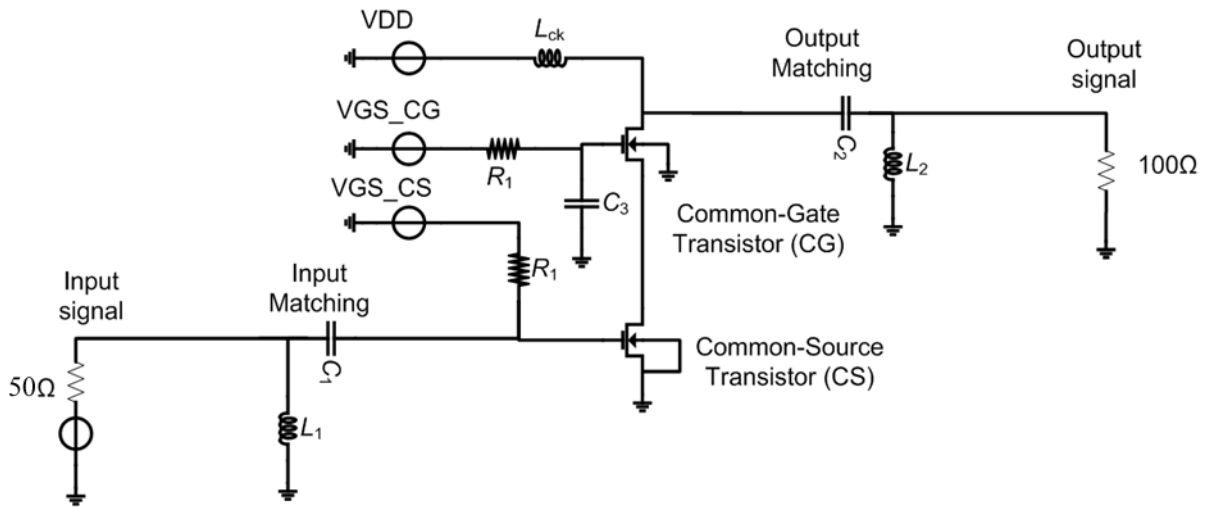


Figure 5.4 – Topology of the cascode sub-PA

Table 5.2 – Optimization variables on the sub-PAs

Ref.	Var.	Variable description	Variable name	Unit
1	Signal source	Maximum input power	Pin	dBm
2	Transistor CG	Drain polarization	VDD_PAx	V
3		Gate polarization	VGS_CG_PAx	V
4		Width	W_CG_PAx	μm
5		Number of parallel devices	M_CG_PAx	-
6	Capacitor CG	Number of fingers on the X direction	nf_cap_CG_PAx	-
7	Transistor CS	Gate polarization	VGS_CG_PAx	V
8		Width	W_CG_PAx	μm
9		Number of parallel devices	M_CG_PAx	-
10	Capacitor C1	Number of fingers on the X direction	nf_dirx_in_PAx	-
11	Inductor L1	Diameter	D_in_PAx	μm
12	Capacitor C2	Number of fingers on the X direction	nf_dirx_out_PAx	-
13	Inductor L2	Diameter	D_out_PAx	μm

Table 5.2 and Table 5.3 present the main variables of the sub-PA design schematic. The name of the variables is presented with an “x” suffix that corresponds to “_PA1” or “_PA2” according to which PA the schematic corresponds. Variables are classified in fixed/adjustable

or optimization variable due to gradient optimization and technology limitations. For each sub-PA, 13 variables were used on the gradient optimizer and six variables were adjusted manually according to reached limits on the other 13 variables.

Table 5.3 – Fixed and adjustable variables on the sub-PAs

Ref.		Variable description	Variable name	Unit
Var.				
1	Signal source	Frequency	Freq	GHz
2	Transistor CG	Number of fingers in CG transistor	nf_CG_PAx	-
3	Capacitor CG	Number of parallel devices	mult_cap_CG_PAx	-
4	Capacitor C1	Number of parallel devices	mult_cap_in_PAx	-
5	Inductor L1	Number of turns	nbt_in_PAx	-
6	Capacitor C2	Number of parallel devices	mult_cap_out_PAx	-
7	Inductor L2	Number of turns	nbt_out_PAx	-

During each optimization stage different methods were used, the gradient, the hybrid and the random method. The gradient optimization evolves fast due to an n-dimension gradient vector created from the optimization variables. The random optimization choses random values inside the variables limits, moving the optimization out of local minimal values, and the hybrid optimization alternate the gradient and the random search.

Many optimization simulations were also done with the genetic algorithm implemented in ADS, however, no results were favorable. The genetic algorithm of ADS was not efficient due to many limitations on its implementation, as for examples, the impossibility to define essential parameters as mutation and cross-over taxes and the size of the population. Other limitation on the stochastic methods on ADS is that many search points can't make the harmonic balance simulation to converge. There is no protection against this problem, when this kind of point is sorted, the simulation return an error and all the process is stopped.

To use the gradient method in an efficient way, it is important to reduce as much as possible the number of variables in the optimization and search in a solution space without local minimum points. Due to polarization restrictions that must be respected, it is possible to considerably reduce the search space. The main PA must work on class B or AB, thus, the possible values for the gate polarization is equal or above the threshold voltage (V_{th}). The

auxiliary PA must work on class C, thus, its gate voltage must be below the threshold voltage (V_{th}). According to PAE and Pout performances and the maximum voltage limits on the transistor, the VDD can be gradually increased (manually) and the PA variables optimized until the circuit reach its maximum performance without surpassing voltage limits.

Optimization schematics created on ADS for the sub-PAs design are capable to produce good results without much time. In a few minutes of optimization, a cascode PA schematic with design kit components can be found with optimized performance and with all restrictions respected. The optimization schematic eliminates many design stages that would be done manually on the conventional methodology and produce better results. The optimization eliminates the load-pull/source-pull loops, the design of the matching networks and fits transistor's sizes and polarizations on the optimum performance.

Main and auxiliary PA performance curves must be plotted on the same graph and analyzed together through the iterations of design for being proper compared until reaching the required shape for making a Doherty with constant PAE performance. Each restriction/objective on the circuit has a weight parameter related to its importance on the optimization. When the number of restrictions and objectives are big, it is normal to reach the final number of optimization iterations with some voltages around the transistor out of the allowed limit. At this point, the weights of these restrictions must be slightly increased and the optimization process repeated. If all restrictions are respected with some distance from the limits but the circuit performance is low, the weights of the restrictions can be decreased and the weights of the performance objectives increased and the optimization process repeated again (Figure 5.5).

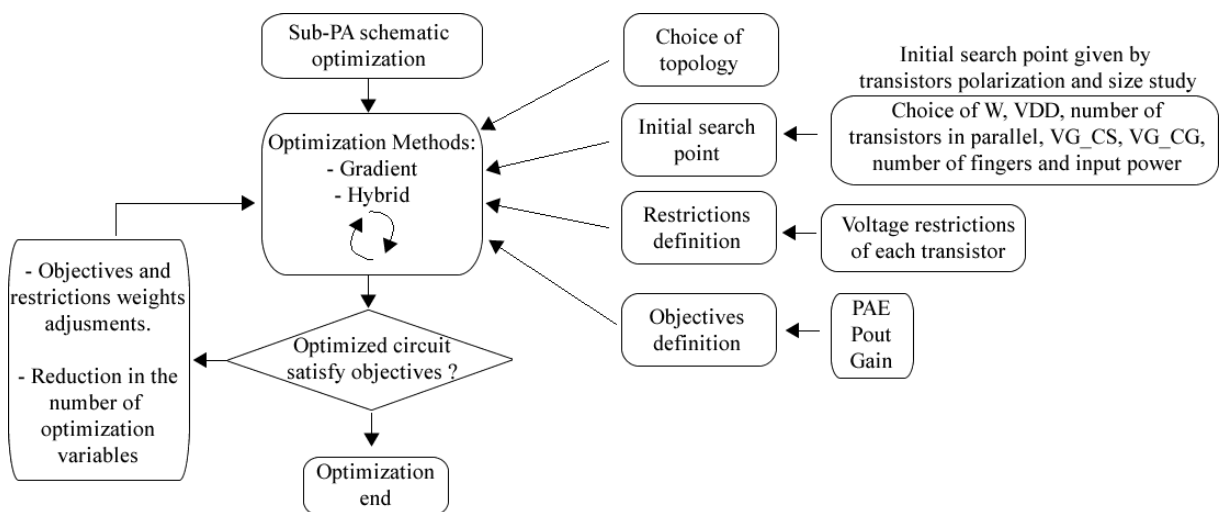


Figure 5.5 – Diagram of the sub PA design optimization schematic.

The designed circuit is composed with transistors with the model next25_hvi (fabricant's CMOS 65nm library), inductors from the family NW (specific group of inductors on the library), MOM capacitors and RPPORPO resistors. The next25_hvi model corresponds to an extended drain high voltage transistor that allows a greater voltage excursion between its poles compared to the others low voltage transistors with model from the fabricant (Design Kit - DK). The schematic symbol of the component is presented on Figure 5.6 and its layout in Figure 5.7. According to the foundry documentation, it supports a Vds voltage excursion of 5.5V, a Vgs of 2.75V and a Vbs of 2.75V. The fabricant does not make reference to the Vgd voltage limit in its documentation, for that reason the limit of 5.5V was considered during the design in according to [66]. The pins sub and siso corresponds to guard rings that must be connected respectively to GND and VDD. The bulk access on the transistor is done by the sub pin. On the schematic the pins bulk and sub are presented in distinct pins but on the layout they are already connected.

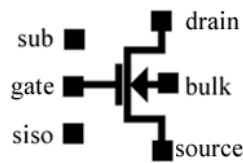


Figure 5.6 – Next25_hvi transistor with its six pins

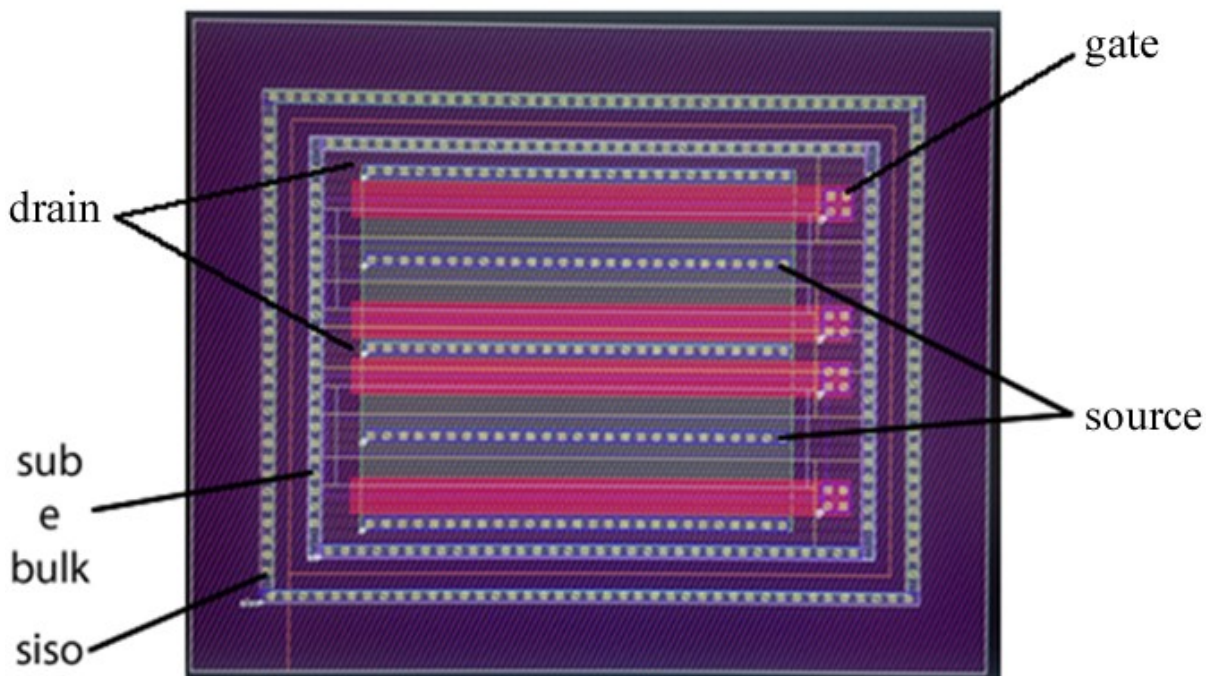


Figure 5.7 – Next25_hvi transistor layout

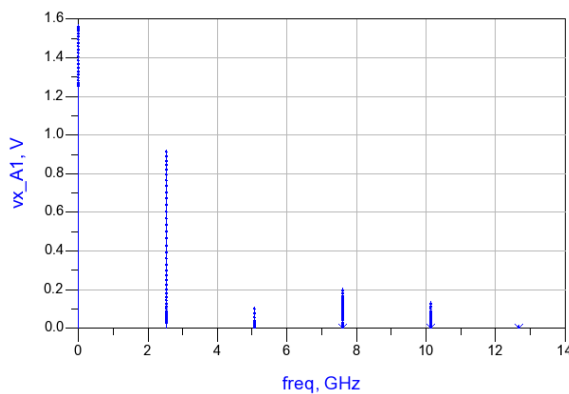
The inductors from the NW family were chosen due to their capacity to reach the desired inductance value yet with a reasonable quality factor (around 10). MOM capacitors were used for being part of the standard options of the technology. The 65nm CMOS component library also provides the MIM capacitors, but special layers must be added on the circuit for their fabrication which considerably increases the cost (more than 7.500 euros/mm² – a quotation must be required for each special option added on the circuit).

The circuit analysis was mainly done with harmonic balance (HB) simulations sweeping the input power of the circuit. After the simulation, transistor voltages are plotted on the time domain (54) (Figure 5.8-b), and then, their maximum and minimum values are plotted versus all simulated input power levels (55) (Figure 5.8-c).

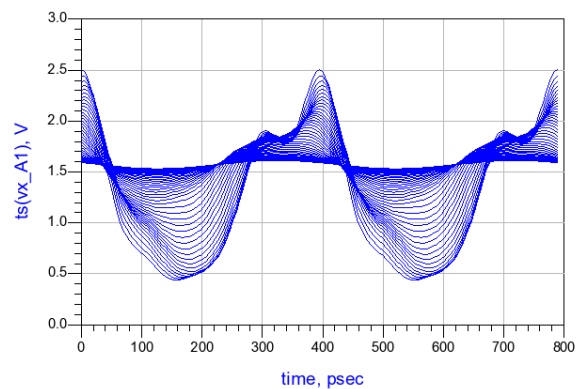
$$V_{GD}(T) = T_s(V_G - V_D) \quad (54)$$

$$\text{MAX}(V_{GD}(T)) = \text{MAX}(T_s(V_G - V_D)) \quad (55)$$

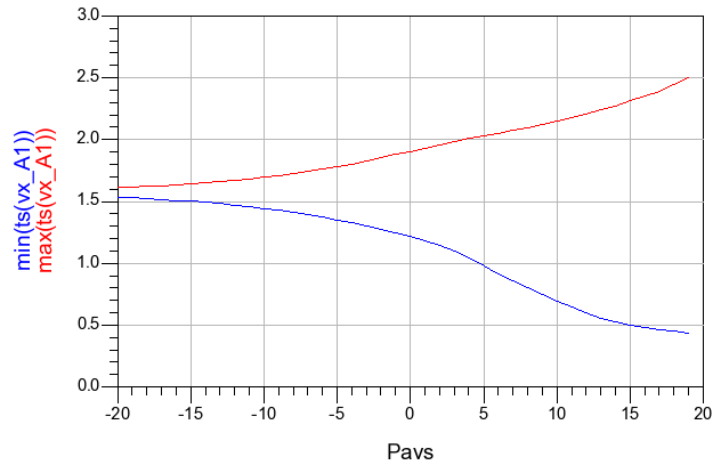
Voltage restrictions on the optimization were the maximum and minimum points of the voltage graph as presented in Figure 5.8-c and computed by equations (56) and (57). The optimization schematic considered 14 restrictions of minimum and maximum voltage to protect the transistor from damage; and one restriction to divide equally the voltage excursion V_{ds} on the transistors of the cascode topology for allowing the maximum V_{DD} . Beyond the restrictions, two others performance variables were added on the objectives, the PAE and P_{out} , according to the Table 5.4. Restrictions have greater weights (Table 5.4) than performance objectives to keep the circuit protect against damage.



a)



b)



c)

Figure 5.8 – Voltage analysis stages. Voltages in frequency domain (a), voltages on the time domain (b), maximum and minimum voltages versus the input power (c)

$$\text{MAXIMUM ANALYZED VOLTAGE LIMIT} = \text{MAX}(\text{MAX}(\text{TS}(\text{VX} - \text{VY}))) \quad (56)$$

$$\text{MINIMUM ANALYZED VOLTAGE LIMIT} = \text{MIN}(\text{MIN}(\text{TS}(\text{VX} - \text{VY}))) \quad (57)$$

The Figure 5.9 shows the ADS optimization cockpit where the evolution of the variables and objective functions can be observed and the optimization algorithm can be changed. It is possible to observe the algorithm convergence and if the objectives have reached a local minimum value.

Table 5.4 – Sub-PAs restrictions and objectives

Ref. restriction	Description	Variable	Condition	Weights
1	Common Gate Transistor	Vgd min	$> -5.5 \text{ V}$	5
2		Vgd max	$< 5.5 \text{ V}$	5
3		Vgs min	$> -2.75 \text{ V}$	5
4		Vgs max	$< 2.75 \text{ V}$	5
5		Vds min	$> -5.5 \text{ V}$	5
6		Vds max	$< 5.5 \text{ V}$	5
7		Vbs min	$> -2.75 \text{ V}$	5
8		Vbs max	$< 2.75 \text{ V}$	5
9	Common Source Transistor	Vgd min	$> -5.5 \text{ V}$	5
10		Vgd max	$< 5.5 \text{ V}$	5
11		Vgs min	$> -2.75 \text{ V}$	5
12		Vgs max	$< 2.75 \text{ V}$	5
13		Vds min	$> -5.5 \text{ V}$	5
14		Vds max	$< 5.5 \text{ V}$	5
15	Both transistors	Voltage division	$V_{ds_CG} = V_{ds_CS}$	5
16	PA performance	PAE	$> 50\%$	2
17	PA performance	Saturation Point	$P_{out} = 15 \text{ dBm}$ $P_{in} = 0 \text{ dBm}$	1

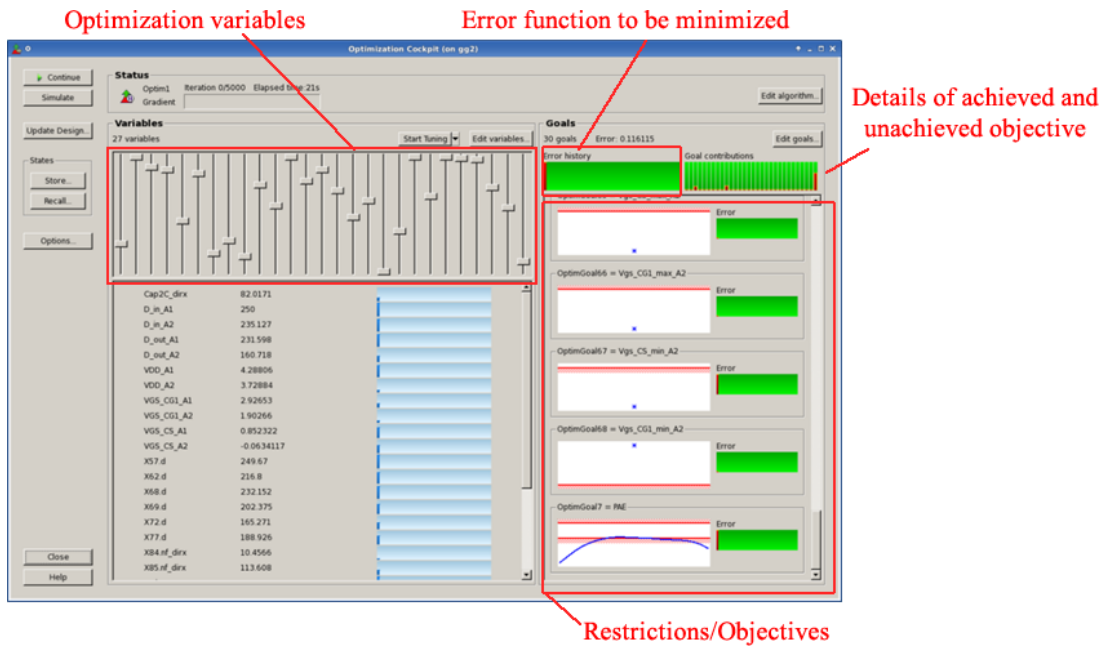


Figure 5.9 – ADS optimization cockpit

It can be observed that some integer variables were used on the gradient optimization algorithm. Simulations demonstrate that the component model accepts real values on the integer variables. On this situation, some components truncate the value (i.e. MOM capacitor) and in other the real value is simulated (i.e. transistor's fingers). One of the disadvantages of the gradient optimization is the convergence to local minimum values; however, this optimization is fast and normally does not generate points that can't be simulated. With this optimization method many periods of manual intervention and optimization can be executed in one journey of work, which is required by most of designers. Stochastic optimization provide the advantage of keeping the algorithm out of local minimum values, however, they need whole days of work without allowing additional intervention of the designer, which is undesirable and generates solution points that can't be simulated by harmonic balance.

The circuit variables were classified in fixed/adjustable and optimization variables due to physical restrictions. In the case of the inductor, the number of turns can't be optimized with the gradient method. In this situation, a determined number of turns is fixed and the diameter is optimized. If the optimization reaches the maximum value of the diameter, the optimization is interrupted and the number of turns is increased for allowing the algorithm to search for higher inductance values. On the case of MOM capacitors that are composed by an integer number of fingers on the X and Y direction, a determined number of fingers is fixed on the Y direction and the number of fingers on the X direction is optimized.

The sub-PAs must be designed for presenting performance curves that when overlapped fits the shapes represented on Figure 5.10. It can be observed that the main PA must be designed to enter on the compression region in a lower output power than the auxiliary PA. The distance in dB between the compression points of both sub-PAs defines the backoff length of the DPA. The maximum output power of the DPA is defined by the addition of the output power of both sub-PAs. The DPA gain performance is composed by two parts, the first is determined by the gain performance of the main PA, the second (on high output power region) is determined by the auxiliary PA gain. The gain and P_{out} levels are defined by the application of the PA (i.e. mobile communication); the PAE level, desired to be as high as possible, is limited by losses from the technology and circuit's topology. When the performances of the sub-PAs reach the behavior presented on Figure 5.10, they can be connected together to compose a DPA.

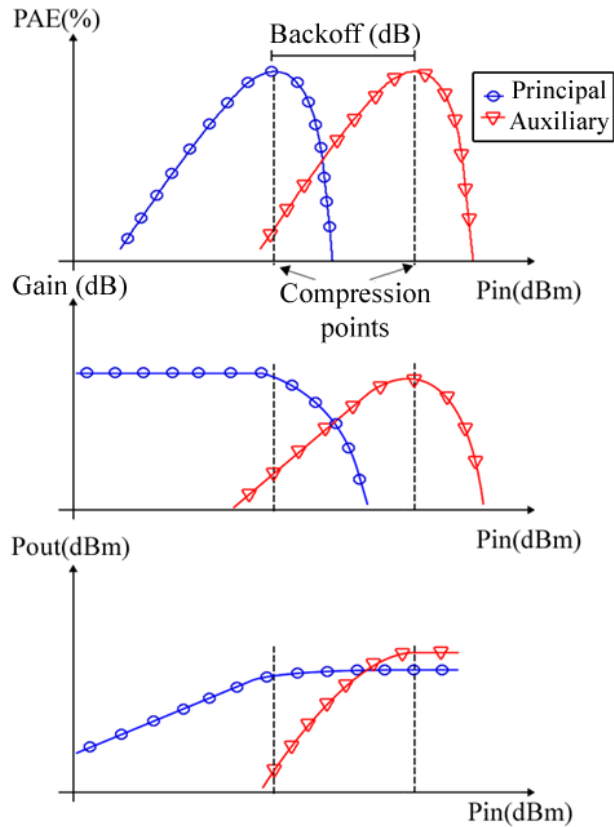


Figure 5.10 – Main and auxiliary PA performance curves of PAE, gain and output power.

5.4.3 Final Individual Design Stage of the Sub-PAs

The sub-PAs were designed and optimized until reaching the PAE, gain and output power performance presented on Figure 5.11, Figure 5.12 and Figure 5.13, respectively. This design stage shows important challenges and limitations of the 65nm CMOS technology and the cascode topology.

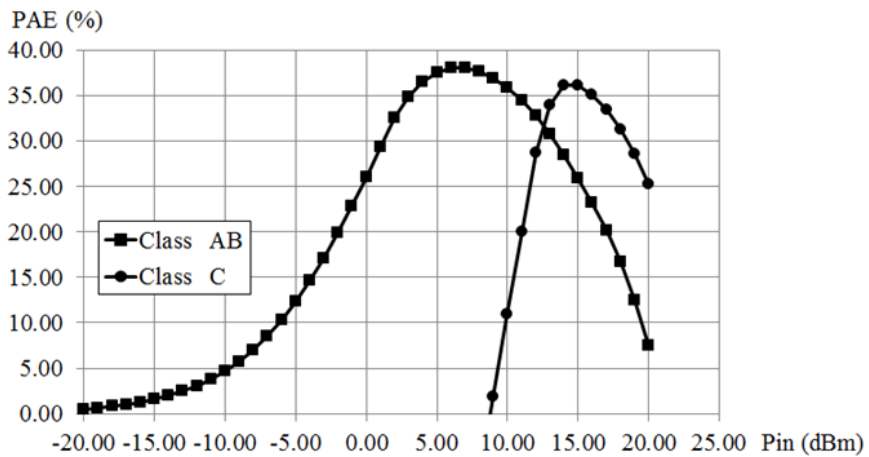


Figure 5.11 – Sub-PAs PAE performance before being connected as DPA

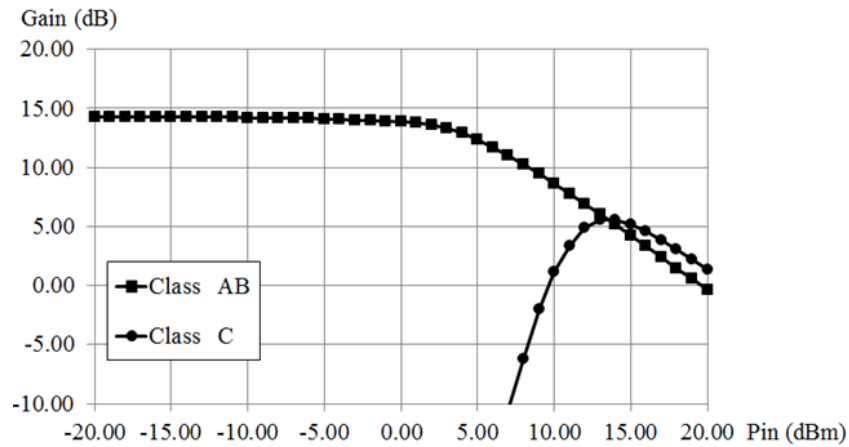


Figure 5.12 – Sub-PAs gain performance before being connected as DPA

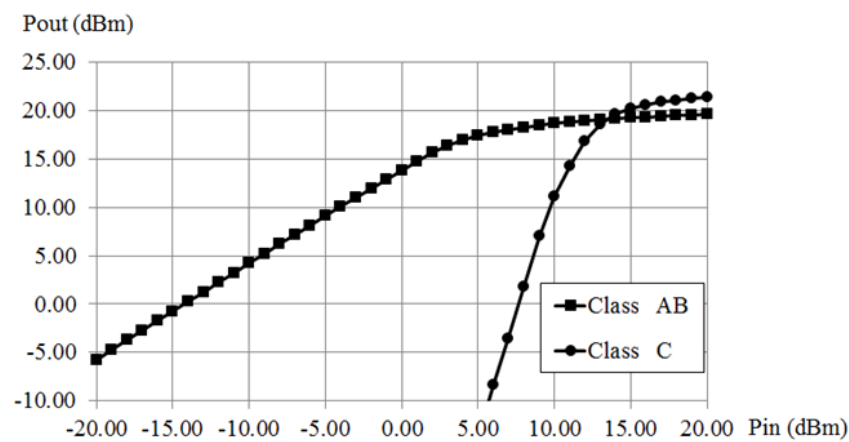


Figure 5.13 – Sub-PAs output power performance before being connected as DPA

It can be observed that the main PA (class AB) presents a considerable high PAE performance and the auxiliary PA (class C) a relative low PAE performance on Figure 5.11. The high PAE value of the main PA was reached because it was designed for a low output power. Studies on the dimension of the transistors showed a potential to produce a maximum output power of 25dBm using the cascode topology polarized on the class AB. Thus, due to the compromise between gain and efficiency, the reduction of output power to 20dBm increased the PAE performance.

The auxiliary PA efficiency is considered low because the class C presents, in theory, higher efficiency than a class AB PA. However, as this PA must get into saturation after the main PA, it must be designed to provide more output power. By “pushing” the class C PA design to provide a high output power (Figure 5.13), its gain is reduced. The lower gain justifies the low PAE performance of the auxiliary PA.

The PAE and Pout performance of the designed sub-PAs present shapes very similar to desired ones in according to Figure 5.11 and Figure 5.13, however, the auxiliary PA (class C) presents a low maximum gain performance on Figure 5.12. For the required output power, the gain of 5dB was the maximum that could be reached within the supported voltage limits of the transistor.

The need for a class C PA that must have more output power than the class AB PA is one of the challenges on the DPA design. The class AB PA reaches easily higher output power due to its higher gate voltage, but, in the DPA, the class AB must get into compression before the class C. The class C PA must produce a higher output power, with the same gain, and get into compression after the main PA (class AB/B), but, due to its low gate voltage it is very hard to reach this objective. As discussed before, the addition of a driver couldn't be a solution on this technology due to the very low efficiency on the auxiliary PA branch.

For reaching a DPA with an output power higher than 23dBm, due to project specifications, it was designed a class C PA with a large transistor which reduced its gain. Due to this deadlock, the priority was given to a DPA with a higher output power (23dBm) and with a constant PAE with the largest as possible backoff rather than the linearity. If the size of both sub-PAs could be decreased, the DPA could be designed with an almost constant PAE and gain, but the output power level would not be reached.

5.4.4 Power Splitter Design

To connect the sub-PAs on the DPA structure a power splitter designed already with fabricant component's models is needed. The Wilkinson power splitter schematic is presented on Figure 5.14 and its design equations in (58), (59) and (60). The power splitter is designed first with ideal components and then they are replaced by components with models from the fabricant. Finally, the schematic is optimized with the objective of equal power dividing and to reduce losses the maximum as possible.

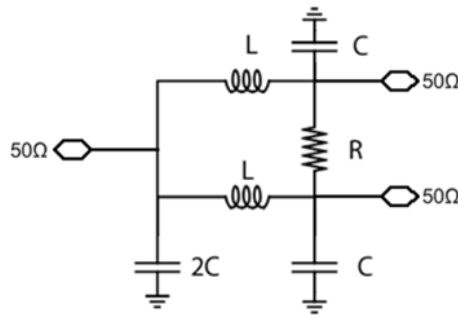


Figure 5.14 – Wilkinson power splitter schematic

$$C = \frac{1}{2\pi f_0 Z_0} \quad (58)$$

$$L = \frac{Z_0}{2\pi f_0} \quad (59)$$

$$R = 2Z_0 \quad (60)$$

5.4.5 Transmission Lines Design and Optimization

The next design stage consists in connecting the sub-PAs with ideal 2-terminal transmission lines (*TLIN* component in ADS) to determine the electric length value of the transmission line of phase correction connected on the auxiliary PA. The important detail to note on this point is that sub-PAs and the power splitter must be already designed with only fabricant components and those they will be connected by ideal transmission lines. Due to the difference of performance between ideal components and fabricant components (model with parasites), it is important to design the DPA with the maximum number as possible of components from fabricant's library and to use ideal components only on critical stages, as the dephasing transmission line. At the end of this stage, the ideal transmission lines are replaced for lumped transmission lines with the PI model.

5.4.5.1 Designing the dephasing transmission line

After connecting the sub-PAs with the power splitter and the two transmission lines as presented in Figure 5.15, a sweep simulation on the electrical length on the transmission line connected to the auxiliary PA input is done.

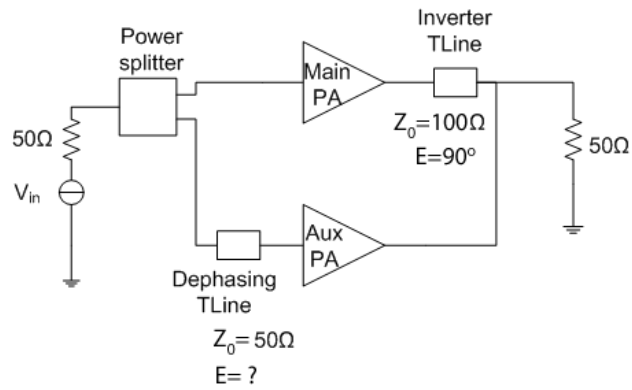


Figure 5.15 – Doherty Power Amplifier simplified schematic

The sweep simulation result must be analyzed by the PAE performance versus the output power, as shown in Figure 5.16. The backoff length of the DPA must be analyzed regarding the output power due to the DPA gain compression. If the backoff is determined by observing the input power, a false larger backoff will be determined.

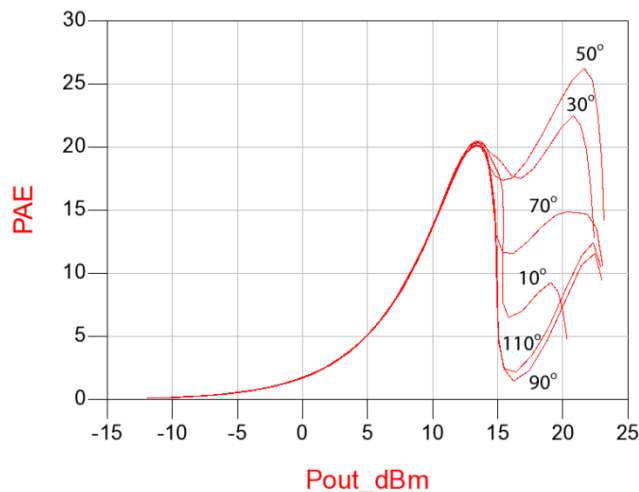


Figure 5.16 – PAE x Pout performance for a sweep simulation on the electric length of the dephasing transmission line

It can be observed on Figure 5.16 that for the correct length, the PAE and output power is increased. Between 10° and 50° the PAE performance increases and between 50° and 110° the PAE performance decreases. The right length value makes the constructive combination of the signals from both sub-PAs. Another sweep simulation must be done with smaller steps to optimize the PAE performance, as presented in Figure 5.17.

It can be observed that the best electric length is of 40°, which is different from the load inverter transmission line that is 90°. It is known that the transistors change the phase in approximately 180°, a value that can suffer some variations with the transistor’s size and polarization. The power splitter and the L network impedance matching on the input and

output also produce differences of phase. By connecting the matching networks on the splitter, its phase values are changed, and the same occurs with the matching networks on the DPA output. Thus, this work found that sweeping the electrical length of the dephasing transmission line is the simplest and best way to determine the correct value, instead of determining the difference of phase produced by each block on the circuit and then adding each value to determine the correct transmission line length, as proposed by [48].

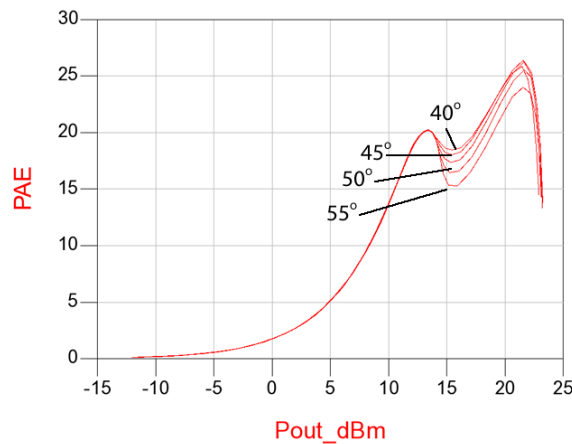


Figure 5.17 – Tuning the transmission line electrical length value

5.4.5.2 Replacing ideal transmission lines by lumped transmission lines

On this design stage the circuit has already both sub-PAs and power splitter with only fabricant components and the constant PAE behavior of the DPA has already being found. However, the circuit has two ideal transmission lines that must be replaced by real integrated components.

Due to the frequency on this design (2.535 GHz) it is not possible to insert on the chip transmission lines with distributed parameters due to its size. The ideal inverter transmission line can be replaced by the lumped PI model as presented in Figure 5.18. The schematic with the result of this substitution is shown in Figure 5.19. The same method can't be applied to the dephasing transmission line because its electrical length is not 90°. To determine correct values for this last transmission line, a PI model is used as in Figure 5.18, all variables of the circuit are fixed and this PI line is optimized. The optimization objective is set for increasing the two peaks of the PAE curve and to make PAE curve more constant as possible inside the region shown in Figure 5.20. As an optimization start point, it is recommended to compute the transmission line values as if it had an electrical length of 90° for reaching faster the final value.

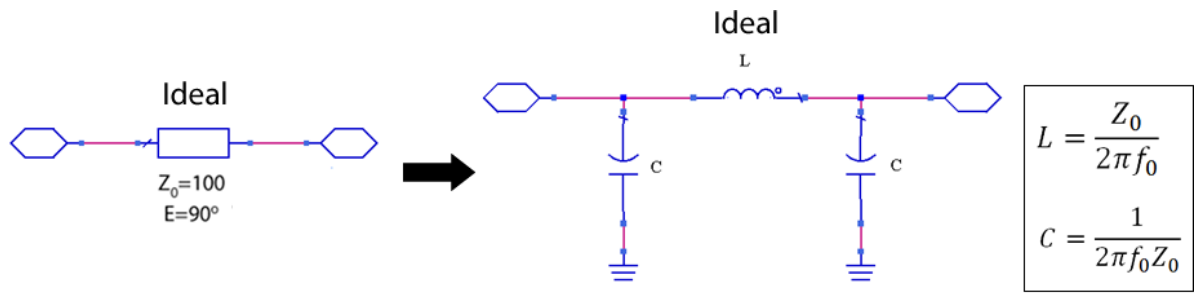


Figure 5.18 – Lumped $\frac{1}{4}$ wave transmission line PI model

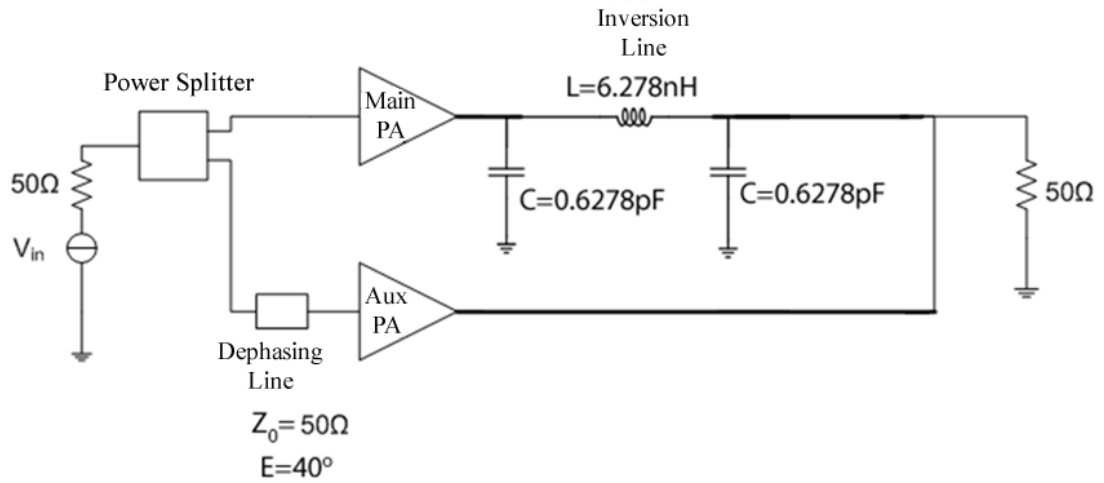


Figure 5.19 – Inverting transmission line replaced by PI model

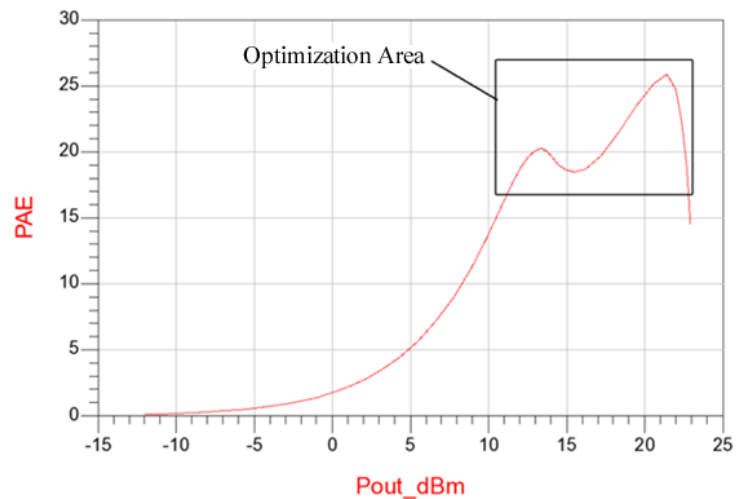


Figure 5.20 – Optimization region

5.4.5.3 Final substitution of ideal components for fabricant components

The final procedure of replacing the ideal components for fabricant components (65nm CMOS technology models from STMicroelectronics) is delicate due to the great difference of performance between them. The Figure 5.21 presents the simplified schematic of the DPA on this stage.

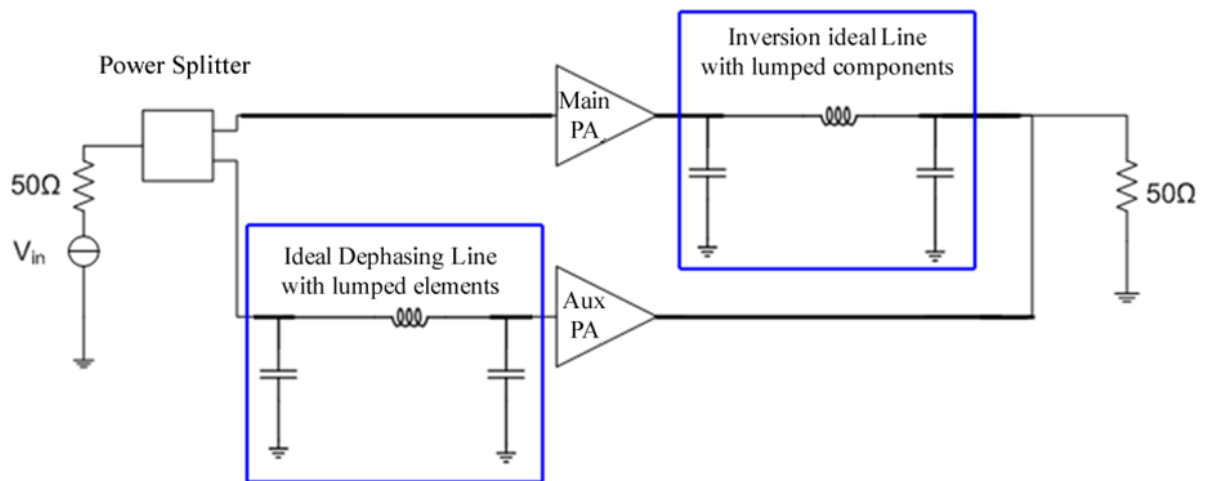


Figure 5.21 – Simplified schematic with lumped ideal transmission lines

It is recommended to replace first the components of the load inverter transmission line and then the components of the dephasing transmission line. This process follows the scheme presented in Figure 5.22. It is recommended to fix all variables on the schematic and optimize only variables of the transmission line. According to Figure 5.22-b, the first component to be replaced is the inductor. The L variable of the ideal inductor is replaced by the variables D (diameter) and $nbtuns$ (number of turns) of the inductor model `indsym_nw_7m4x0y2z_acc`. It was used for the inductor path the maximum width ($11.99\ \mu\text{m}$) for supporting high currents, giving priority to the robustness and reliability instead of the quality factor.

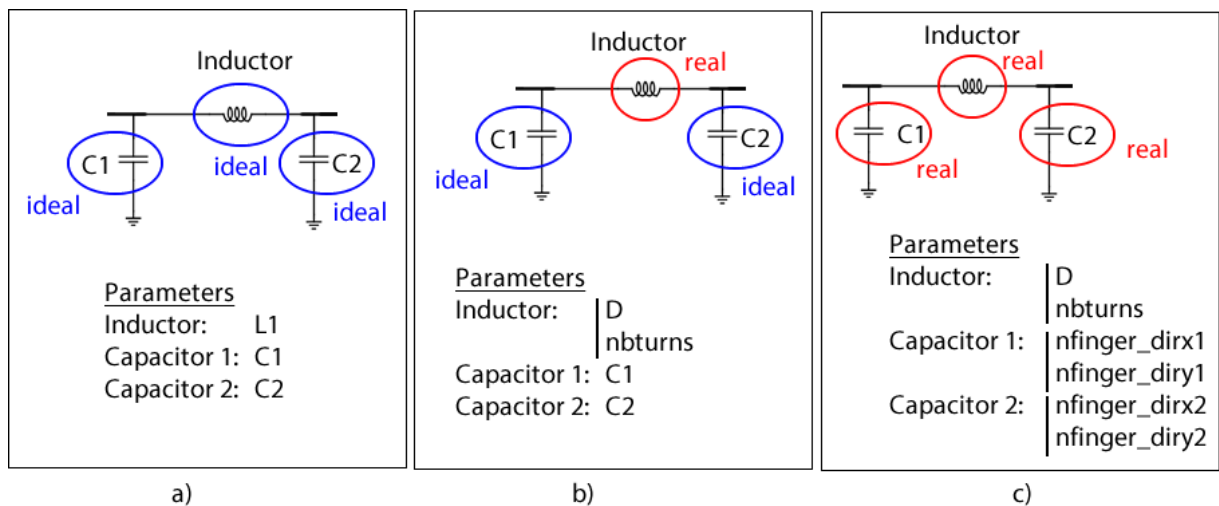


Figure 5.22 – Components replacing sequence. a) First stage. b) Replacing the inductor. c) Replacing capacitors.

The inductance values of NW inductor family can be directly obtained from CADENCE design environment or from the Inductor Selector Program provided by STMicroelectronics.

A wide range of inductance values can be reached with the inductor NW family, going from 0.7nH (with two turns, 11.99 μm path width and 90 μm of diameter) until 17.11nH (with six turns, 8 μm path width and 250 μm of diameter) taking an area of 550 μm per 560 μm on the chip.

By replacing the ideal inductor for a inductor with a model from the fabricant with the same inductance value it can be observed that the PAE sharply changes. The elements of the transmission line must be optimized with the objective to recover the PAE performance before the replacement and with constant behavior.

After this optimization stage, ideal capacitors must be replaced by MOM capacitors. The capacitance value C is replaced by the number of fingers of the capacitor on the X and Y directions and the number of capacitors in parallel because one single MOM capacitor on its maximum size can reach the maximum capacitance of 4.32 pF with 306 fingers on the x direction and 150 fingers on the y direction, taking the area of 33 μm per 70 μm . This type of capacitor also needs many metal levels, normally going from the M2 layer until the M5 layer. Before replacing capacitors another optimization process must be done to recover again the PAE performance. The same methodology of replacing components and optimization is used for the dephasing transmission line.

At the end of this stage, the schematic is composed by only fabricant components. All variables of the circuit must be enabled for optimization and a new optimization process must be done due to increase the PAE, output power and gain performance. The Figure 5.23 presents the whole schematic of the circuit at this design stage. It is important to note that on this moment the gradient optimization process becomes heavy (i.e. one or two days of simulation) due to the great number of variables and restrictions, however, it is possible yet to increase the performance of the DPA. The Figure 5.24 presents the DPA performance at the end of this stage.

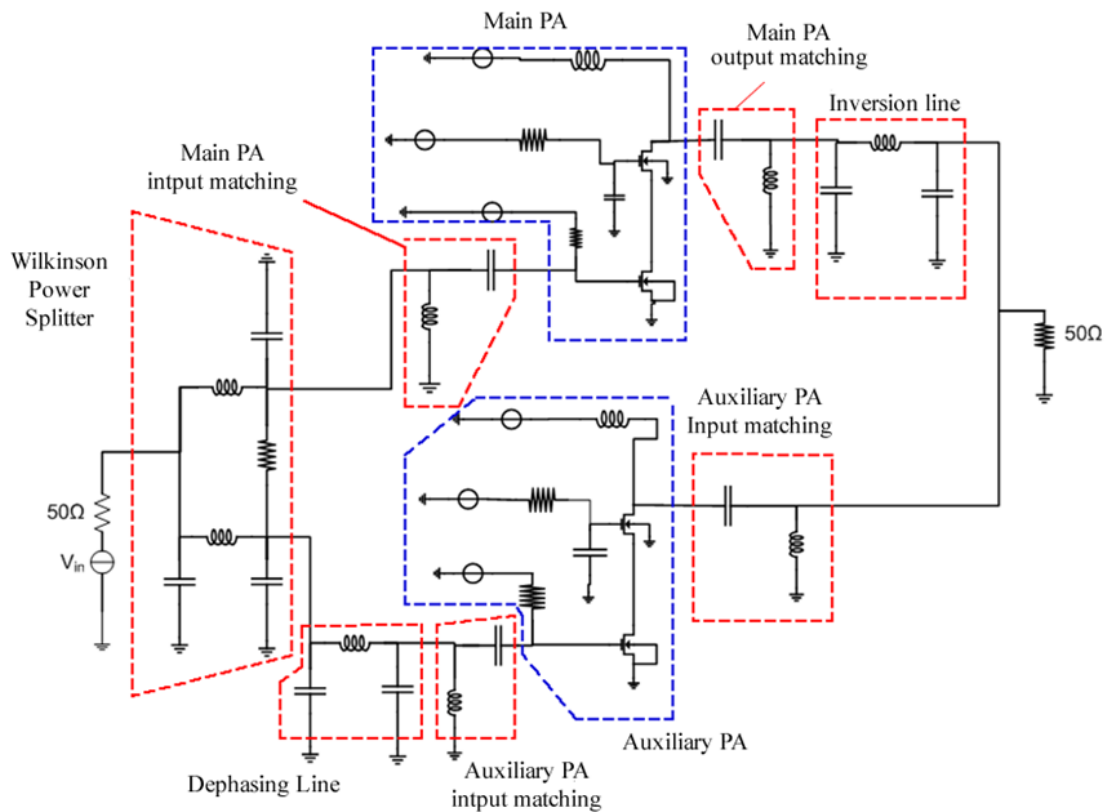


Figure 5.23 – Detailed topology of the DPA with only fabricant components

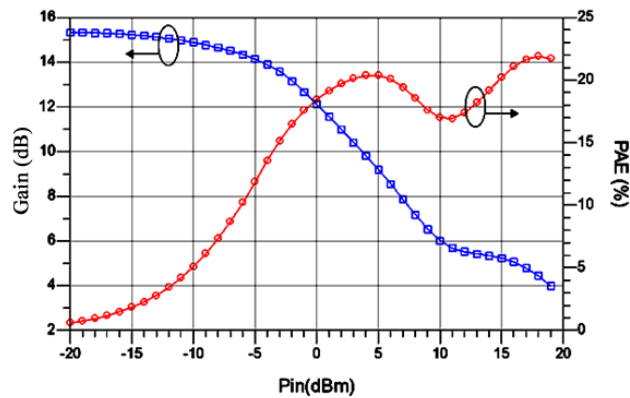


Figure 5.24 – Performance of the Doherty Power Amplifier

5.4.6 Layout Pre-Analysis

Since the circuit has only fabricant components it is possible to make a superficial analysis on the chip required space. By inserting all its components on the layout it can be estimated a chip area around 4.9mm^2 ($3.08\text{mm} \times 1.58\text{mm}$), as can be seen in Figure 5.25.

The prototype cost of integrated circuits on the 65nm CMOS STMicroelectronics technology depends on the chip area. This technology permits the use of 10 metal layers and MIM

capacitors which increases the performance, but also considerably increases the costs. Thus, all effort must be done on the way of reducing the chip size and to use only standard options.

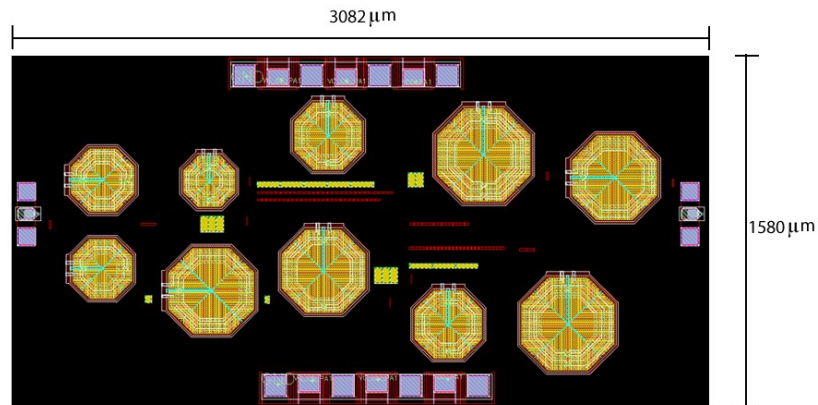


Figure 5.25 – Chip area estimation

5.4.7 Input and Output Network Matching Optimization for Chip Area Reduction and the Final Schematic Details

After connecting all blocks of the circuit, it can be observed that there are inductors in parallel with capacitors. When this structure is on the circuit there is the possibility to exclude inductors and/or capacitors and to keep a good matching by re-sizing other components of the network.

According to Figure 5.26, it was excluded one inductor and one capacitor that were part of the network matching of the main PA and the inverter transmission line. With the same technique, a capacitor and an inductor from the dephasing transmission line and the input network matching of the auxiliary PA were excluded. One capacitor that was part of the power splitter and another of the dephasing transmission line were merged, a capacitor from the superior part of the power splitter were excluded by resizing the inductor in parallel that composes the input network of the main PA and the resistance of decoupling of the splitter was also excluded.

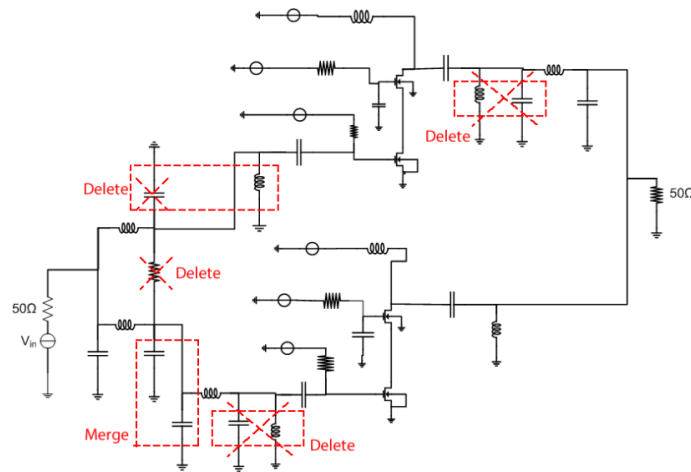


Figure 5.26 – Input and output network matching optimization

All changes on the circuit were applied carefully and one at each time. For each changed component, the PAE performance was degraded and then an optimization was done for changing the network matching and recovering the previous performance. The Figure 5.27 presents the final topology of the circuit. It can be observed that there is yet the inductor L5 in parallel with the capacitor C4. If the capacitor C6 could be eliminated, the inductance L5 and L6 could be merged in just one, however, these changes were attempted but the PAE constant performance could not be recovered, so these components remained as they are.

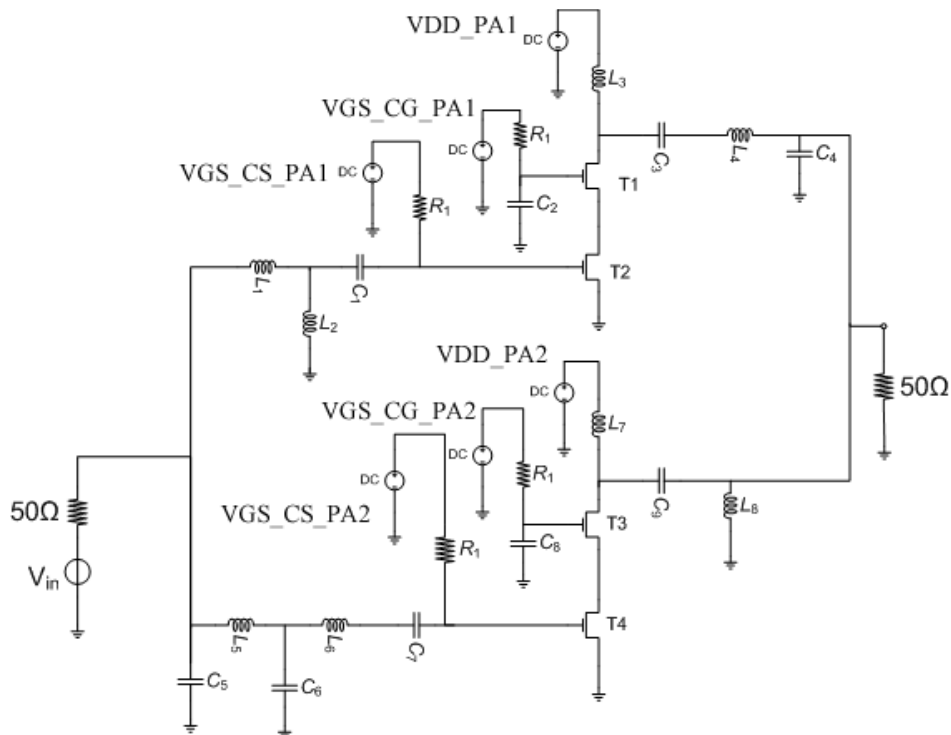


Figure 5.27 – Final topology of the circuit

Figure 5.28 and Figure 5.29 present the PAE and gain performance before and after the topology change and sequential optimizations. It can be observed that beyond saving chip [67] area (by reducing the number of inductors) it was possible to increase the circuit performance. It can be observed a mean increase of 5% of PAE and 3dB of gain (the double) on the small signal region. This increase of performance was due to the reduction of losses caused by each eliminated component. It is presented on the following tables all details of circuit components for further implementations (Table 5.5, Table 5.6, Table 5.7, Table 5.8 e Table 5.9).

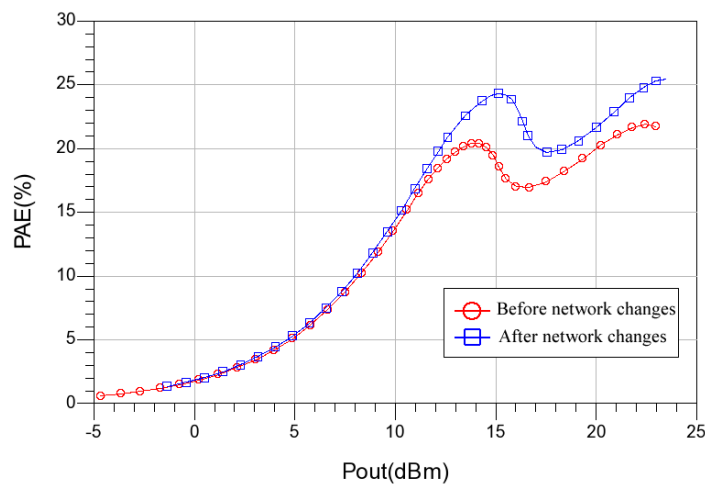


Figure 5.28 – Increase on PAE performance due to changes on the input and output networks

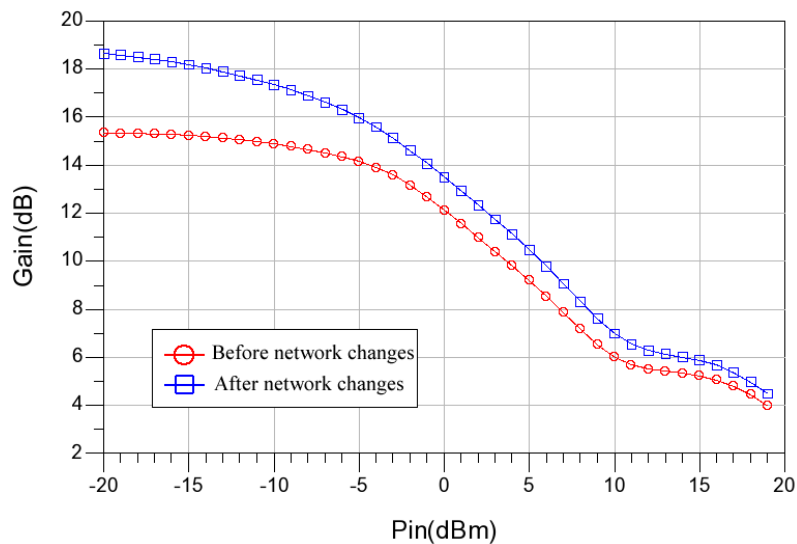


Figure 5.29 - Increase on Gain performance due to changes on the input and output networks

Table 5.5 – Resistors

Ref. resistor	Individual value	Dimensions (μm)	
		W	L
R1	1.997 k Ω	5.0	14.12

Table 5.6 – Capacitors

Ref. capacitor	Individual value	N° of fingers		N° of parallel devices	Total Value
		Direction x	Direction y		
C1	4.31 pF	305	150	3	12.93 pF
C2	4.27 pF	454	100	5	21.35 pF
C3	3.86 pF	273	150	2	7.72 pF
C4	1.365 pF	10	148	1	1.365 pF
C5	2.336 pF	25	100	1	2.336 pF
C6	1.993 pF	143	148	1	1.993 pF
C7	4.31 pF	305	150	3	12.93 pF
C8	4.155 pF	441	100	3	12.465 pF
C9	0.633 pF	45	150	2	1.266 pF

Table 5.7 – Inductors

Ref. inductor	Value	N° of turns	Path width (μm)	Diameter (μm)	Length (μm)
L1	2.44 nH	3	11.99	147.2	2096.17
L2	1.54 nH	3	11.99	93.42	1561.53
L3	2.76 nH	3	11.99	165.00	2273.12
L4	4.17 nH	3	11.99	239.08	3009.56
L5	2.15 nH	3	11.99	130.54	1930.55
L6	4.31 nH	3	11.99	245.88	3077.16
L7	2.76 nH	3	11.99	165.00	2273.12
L8	7.10 nH	4	11.99	233.26	4219.82

Table 5.8 – Transistors

Ref. transistor	Dimension** (μm)		N° of fingers	N° of parallel devices
	W	L		
T1	41.56	0.25	4	28
T2	41.72	0.25	4	26
T3	69.69	0.25	6	26
T4	99.81	0.25	6	14

** The total W is divided by the number of fingers.

For example, W=40 μm and 4 fingers means that each finger has 10 μm length.

Table 5.9 - Polarization

Source	Voltage (V)
VGS_CS_PA1	0,8
VGS_CG_PA1	2,55
VDD_PA1	3,21
VGS_CS_PA2	-0,10
VGS_CG_PA2	2,36
VDD_PA2	4,54

The DPA small signal simulation (S-parameter) results are shown in Figure 5.30. The small signal simulation in a PA is normally used to analyze the matching network. It is done by verifying if the gain peak is centered on the frequency of the project. In the DPA, this analysis provides more interesting information when compared to measurements results, which helps to solve design problems. As the DPA is designed to work on the high output power region (large signal), where the PAE is constant, and as its network matching changes dynamically with the signal increase, the positioning of the gain peak out of the design frequency (2.535 GHz) on the small signal region does not present much significance.

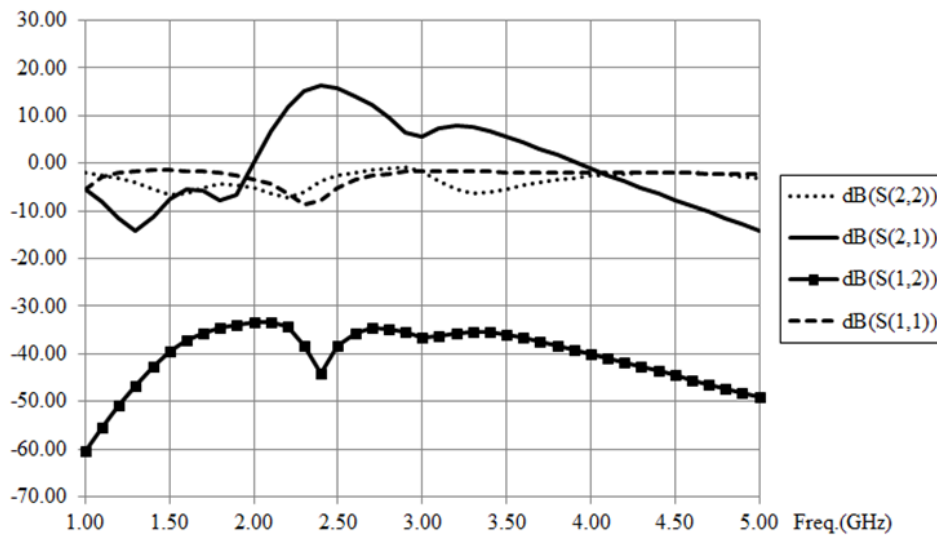


Figure 5.30 – S-parameter simulation of the DPA schematic

The Figure 5.31 presents the PAE and gain performance of the DPA and a class B PA (also designed on the CMOS 65nm technology). It can be observed an increase of 15% of PAE on an 8.75dB output power backoff in relation to the class B PA.

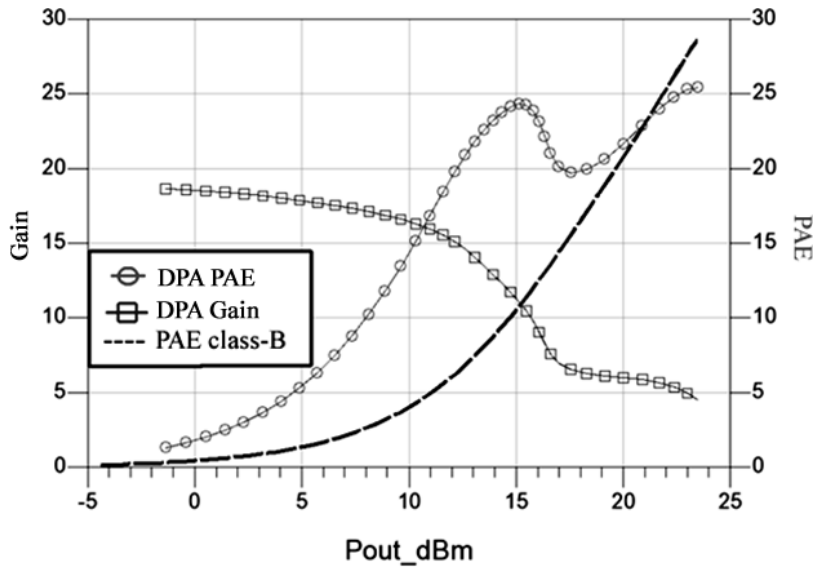


Figure 5.31 – PAE and gain performance of the DPA schematic and the PAE performance of a class B PA schematic

The Figure 5.32 shows the drain constant voltage and load modulation behavior on the drain of the main PA as proposed by the DPA theory. The Figure 5.33 presents sub-PAs output current behavior and the DPA PAE performance.

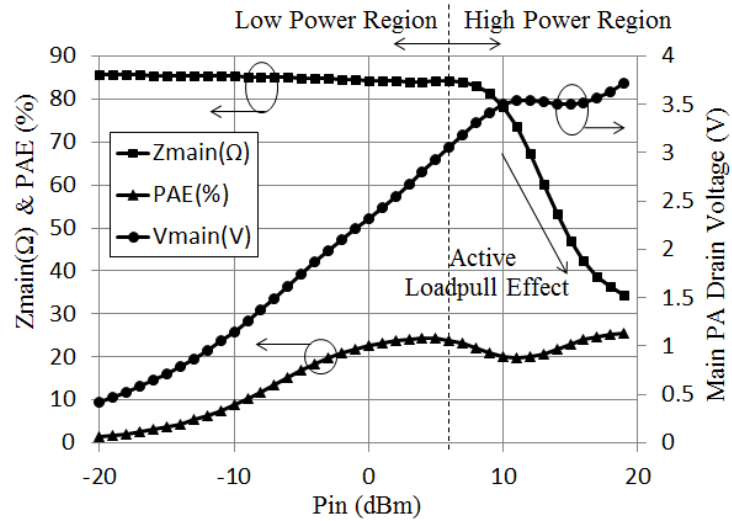


Figure 5.32 – Load modulation (Z_{main}) and constant voltage (V_{main}) on the main PA drain

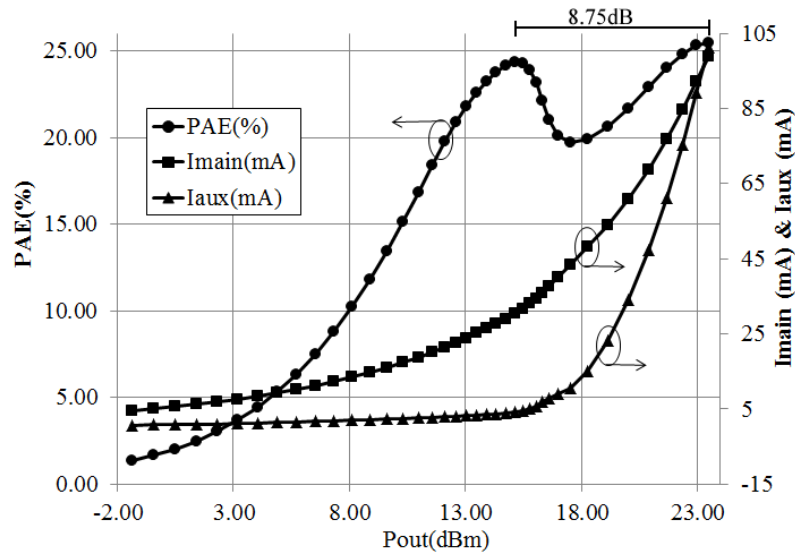


Figure 5.33 – Main PA and auxiliary PA output current behavior (current peak magnitude versus the input power) and DPA PAE.

The Table 5.10 and the Table 5.11 show the voltage level of VDS, VGS, VGD and VBS on the common-source (CS) transistor and common-gate (CG) transistor of the main PA and auxiliary PA and the Monte Carlo simulations for the technology variations modeled by the fabricant. The center value corresponds to nominal simulated values. It can be observed that for nominal voltages transistors still inside supported limits. For Gaussian modeled variations, there is a higher probability to fabricated device to be near the central values. For some simulated variations (with less probability to occur) the voltage surpasses the security limit. The DPA was designed to work until a maximum input power of 19dBm. Figure 5.34 shows a failure test in relation to technology variation done by Monte Carlo simulations for performance variations. It can be seen that the two peak shape for the PAE performance remains in a robust way but the gain performance is quite sensible because of the great impact of variations on the auxiliary PA gate and the appropriate synchronized behavior between each sub-PA. As small changes on the transistor's V_t can produce high variations on the gain, variations on the circuit polarization during measurements can be predicted.

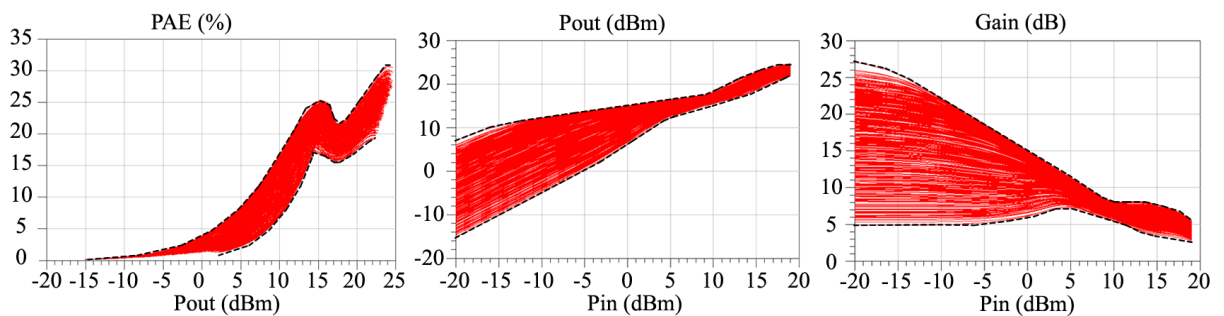


Figure 5.34 – Monte Carlo simulations for performance variation

Table 5.10 – Main PA voltages and Monte Carlo simulations

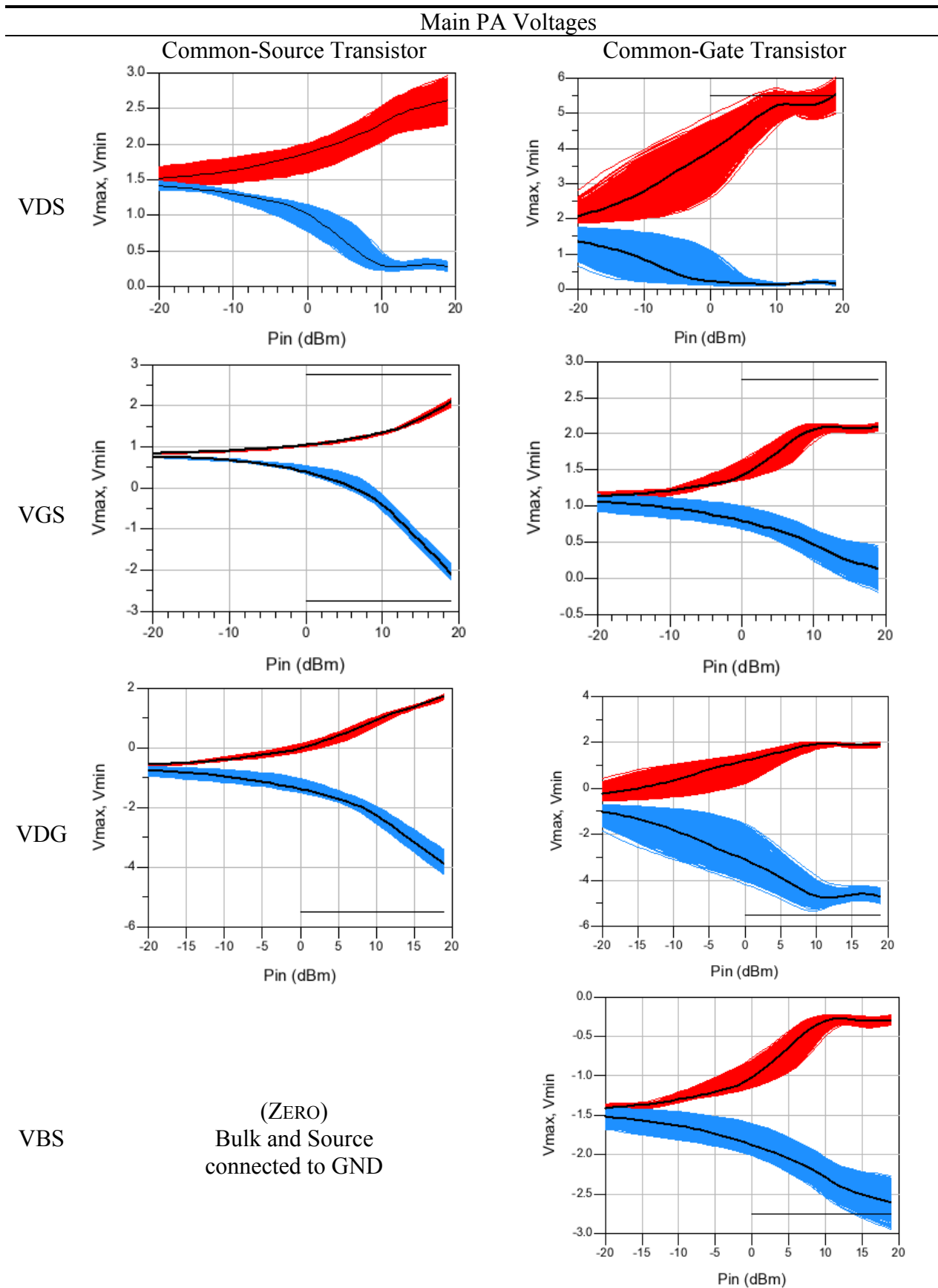
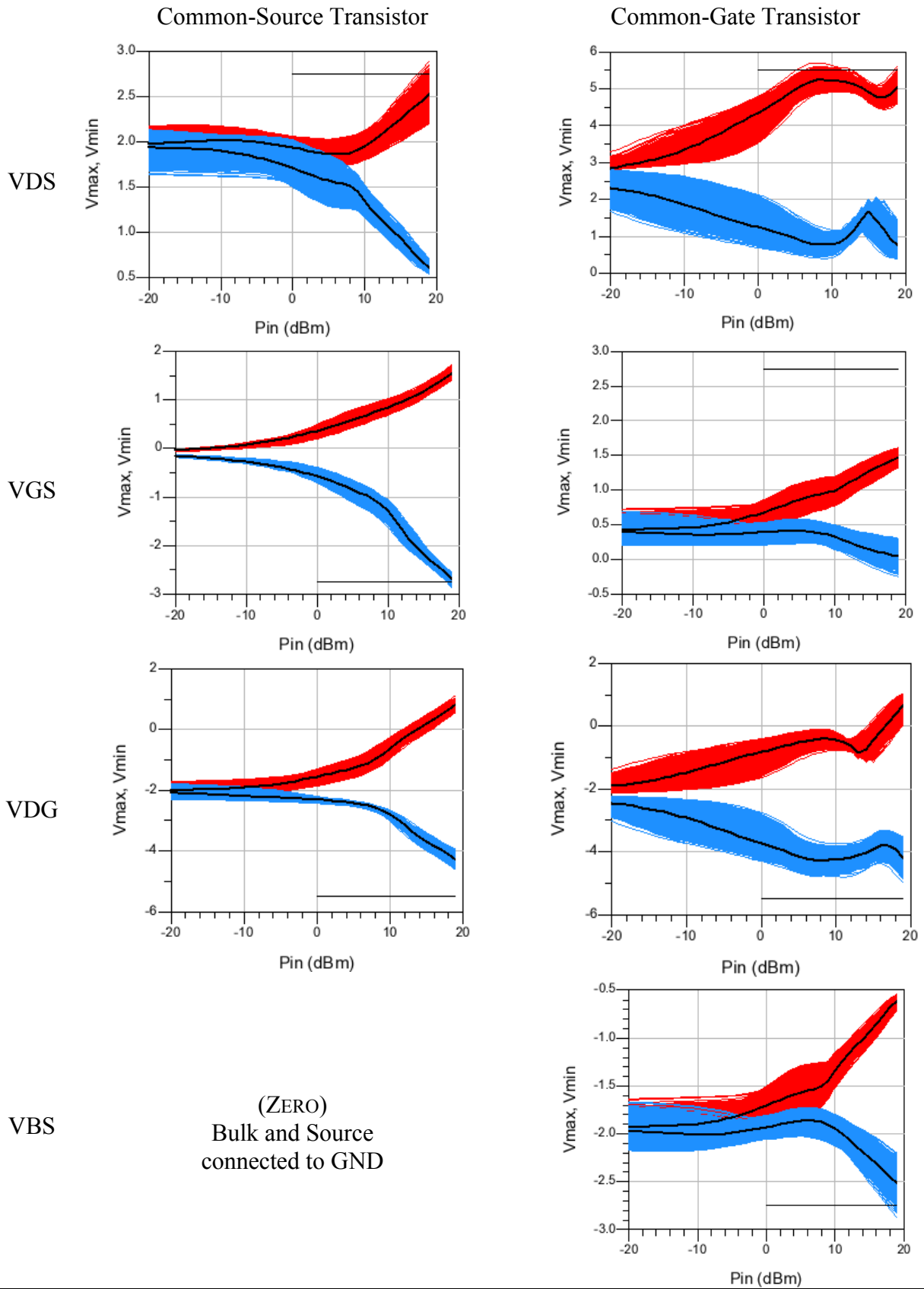


Table 5.11 – Auxiliary PA voltages and Monte Carlo simulations

Auxiliary PA Voltages



5.4.8 Performance Validation on CADENCE schematic

Switching of design software can produce changes on the simulated performance in some cases depending on Design Kit library. Different libraries must be done for each design environment (i.e. CADENCE, ADS) and the great number of versions released by the fabricant may change the performance of the circuit even if it is of the same technology.

The ADS capabilities are better suited for schematic design and optimization and CADENCE is better suited for layout design. The CMP enterprise and STMicroelectronics foundry also checks DRC rules and demands files generated from CADENCE, so, on the final stage of implementation this software must be used to validate the circuit. In according to Figure 5.35 and Figure 5.36 the simulation of the DPA schematic in CADENCE validates the performance presented before.

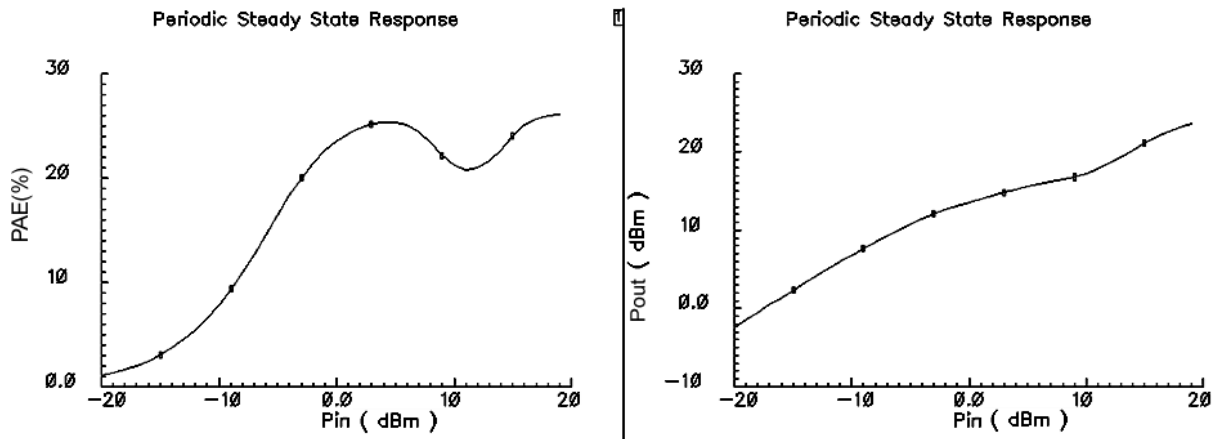


Figure 5.35 – PAE and Pout performance versus input power in CADENCE

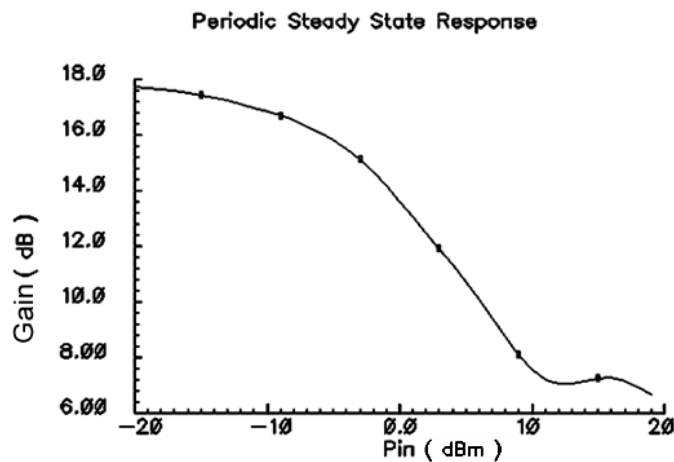


Figure 5.36 – Gain performance versus input power in CADENCE

5.4.9 Layout Details and Post-Layout Simulation Results

The designed DPA was fully integrated on 65nm CMOS STMicroelectronics technology [68]. The layout sent to fabrication presents an area of 2.9 mm² (1720μm×1680μm) and it is presented on Figure 5.37. The figure indicates the function of each PAD and each polarization voltage level.

As can be seen, RF pads were positioned on the left and right border of the chip, and bias PADS on the top and bottom. It can be noted some space at the top and bottom of the chip that could place the RF PADS but during measurements different pointers are used for RF signal excitation and DC supply and them can't be placed side by side (with a reasonable distance for a chip).

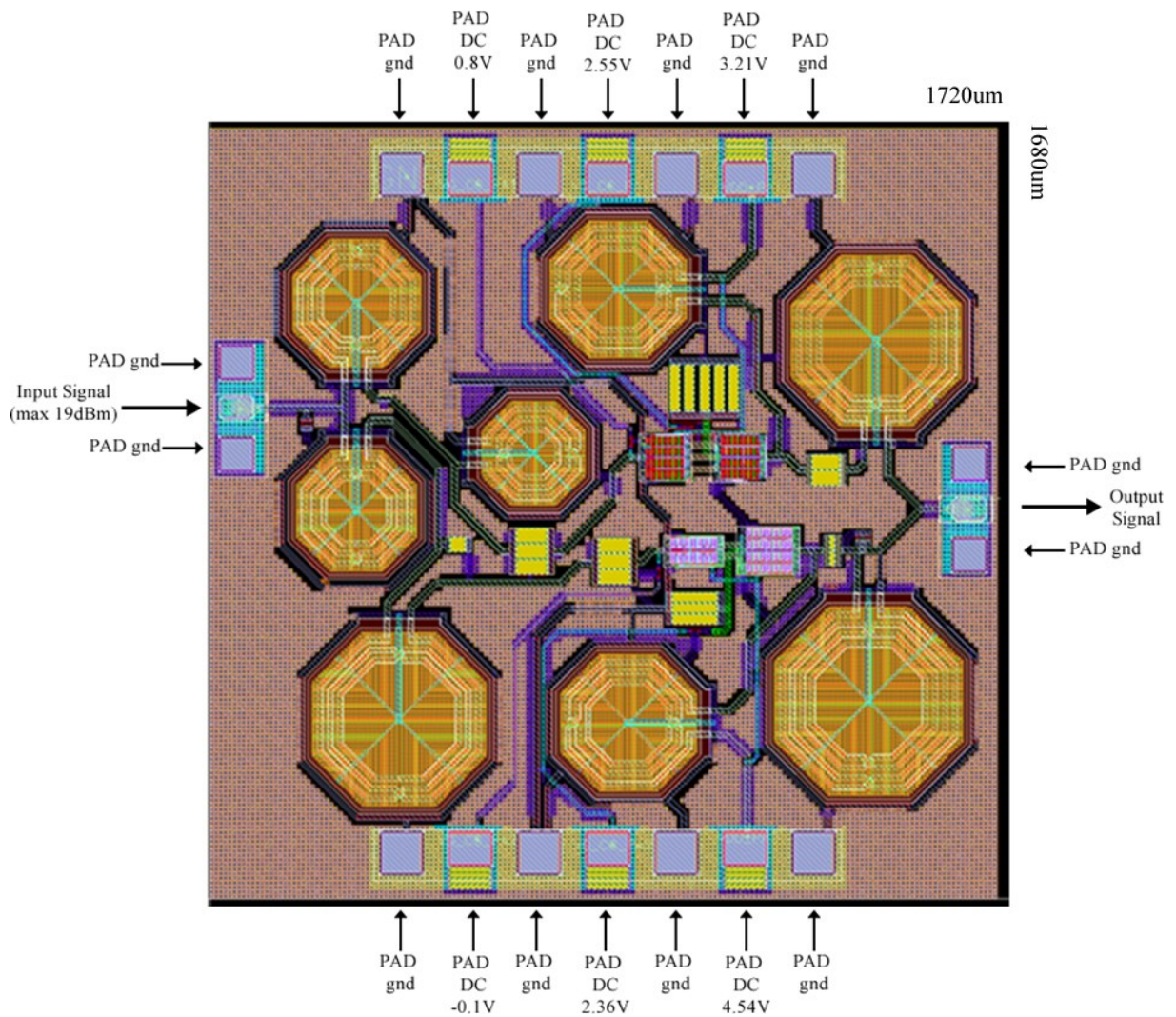


Figure 5.37 – Doherty Power Amplifier layout sent for fabrication

The Figure 5.38 presents small signals (S-parameters) post-layout simulation results and the Figure 5.39 presents large signal (harmonic balance) simulations results. A performance decrease can be observed in relation to the schematic simulation due to losses and mismatching caused by parasitic resistances and capacitances considered only on the layout. However, the constant PAE performance, that represents the main objective of the design, can be observed on the large signal simulation. Further comparisons between layout and schematics are done on the result analysis section.

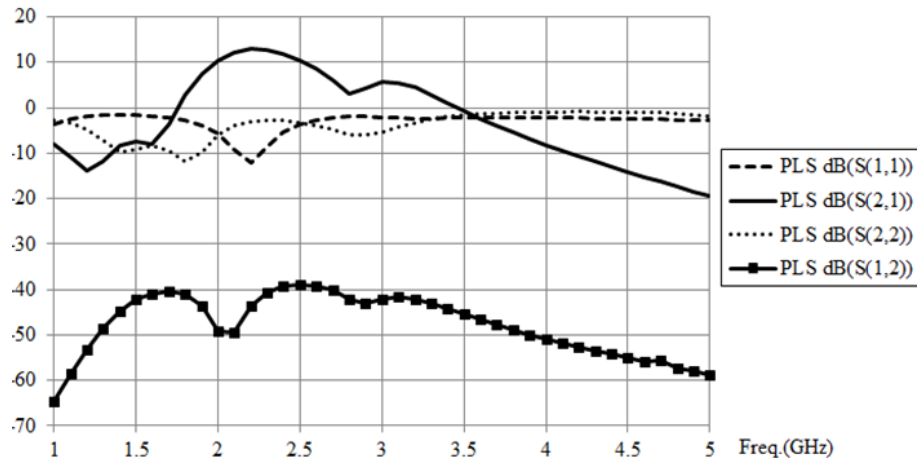


Figure 5.38 – Post-layout S-parameters simulation

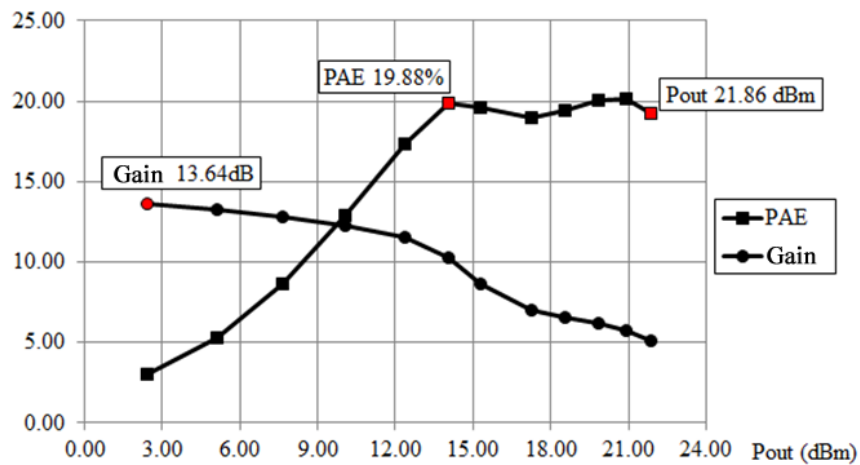


Figure 5.39 – Post-layout large signal performance simulation

The Figure 5.40 shows paths for the RF signal (P1-P12) (left) and paths for gates and drains polarization, and transistor’s guard rings (P13-P20) (right).

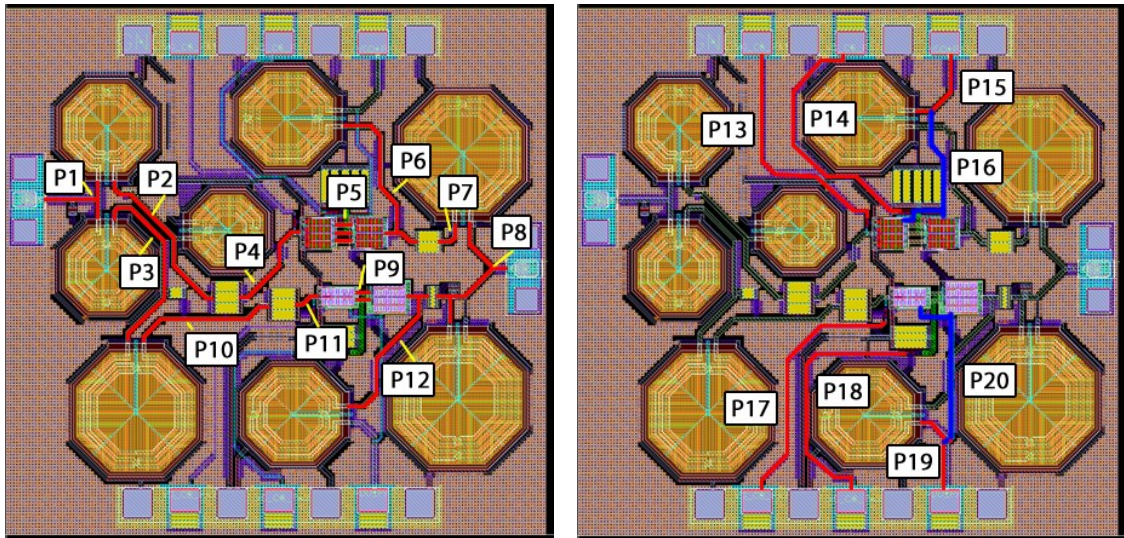


Figure 5.40 – Signal path highlighted

Each group of transistors was designed with an analog shape as shown in Figure 5.41. It can be observed that each transistor from schematic is composed by many small transistors in layout with small fingers.

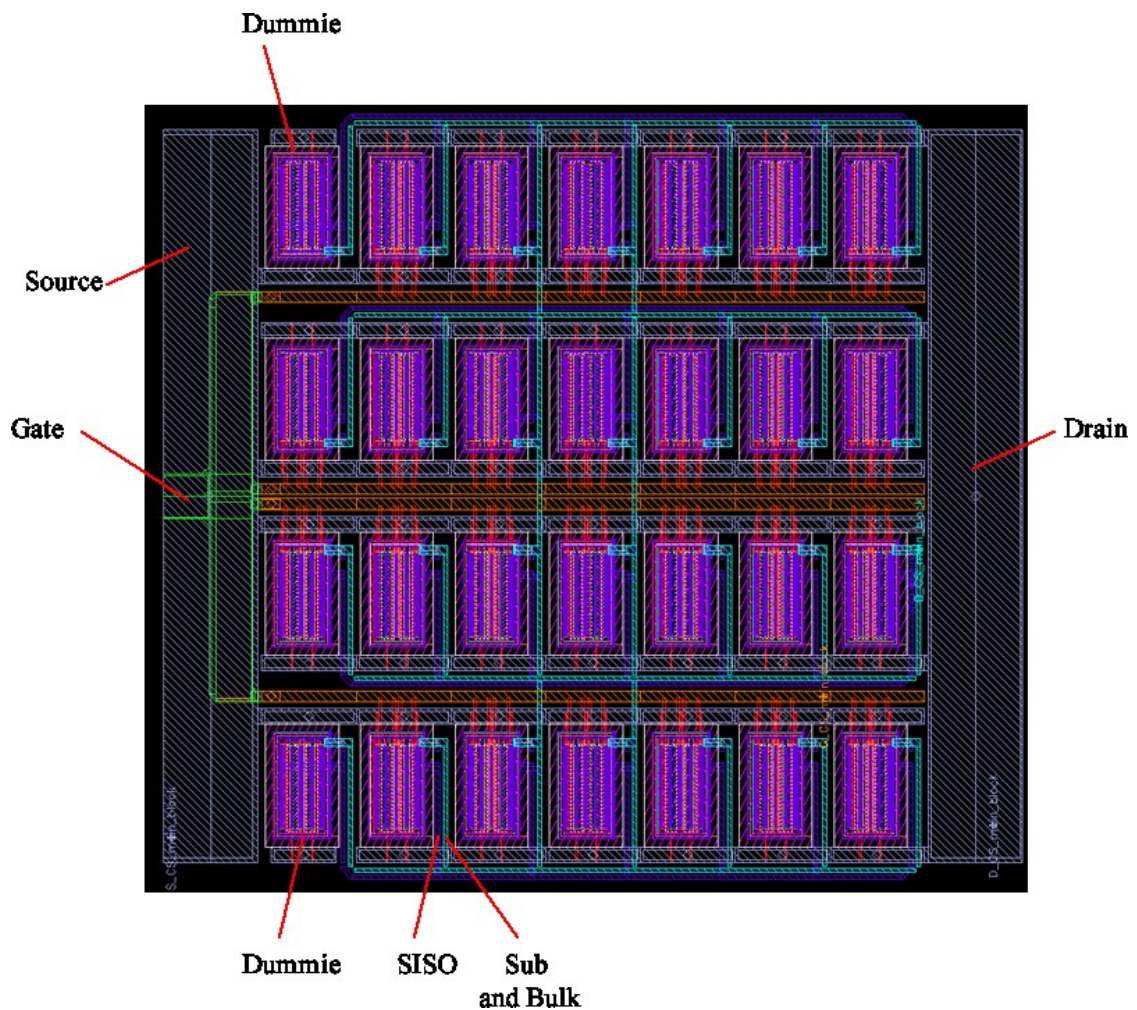


Figure 5.41 – Position and organization of adjacent transistors in layout

It can be observed in the periphery of the chip (Figure 5.37 and Figure 5.40) a thick metal that composes the ground plane. All PADS with GND voltage reference are connected to this plane. It is composed by small cells of 10 μ m by 10 μ m, each one with seven metal layers connected and stacked. This ground plane was designed with the objective to completely cover the substrate to avoid effects on the signal by substrate currents and to produce a robust block for making a consistent ground reference.

5.4.10 Circuit Re-optimization with Layout Parasites

As presented in previous sections, there is a performance reduction between post-layout simulation and schematic simulation due to parasitic resistances and capacitances from layout paths and that are not considered in the schematic. This loss of performance is variable and depends on geometric details of the layout. The post-layout simulation helps to anticipate the circuit measured performance; however, CADENCE parasites extraction normally recognizes only parasites resistance and capacitance.

Parasitic resistances reduce the performance due to heat dissipation and parasitic capacitances produce losses due to mismatching. The fact of ignoring paths parasitic inductances and mutual inductances between paths and inductors makes the post-layout simulation to present matching results considerably different from reality.

Beyond the methodology of DPA design with sequential optimizations, this work proposes also a circuit optimization using electromagnetic models made from layout paths. In that way, all layout connections must be modeled with an electromagnetic simulation due to consider parasitic and mutual inductances. The circuit can be re-optimized to resize lumped components to mitigate the mismatch problem and to higher the overall performance.

5.4.10.1 Electromagnetic Simulation and Paths Modeling

The creation of electromagnetic models for layout paths starts by exporting each path from layout view, in the “.gds” format, and by importing them in an electromagnetic simulator (MOMENTUM, in our case, which works inside ADS design interface). ADS paths importation must be done together with metal layers and substrate technology parameters. Next, the great number of vias in layout paths must be simplified for having a feasible

electromagnetic simulation time. It is done by replacing groups of vias by single blocks to represent their connections. Finally, input current on paths must be represented by “Ports” components properly configured for each kind of connection. Paths very close from each other must be modeled together to represent their coupling. Blocks generated by the electromagnetic simulation are described by S-parameters. In this project, models were done by simulations up to 13GHz (with 50MHz linear steps) due to consider effects up to the fifth harmonic (design frequency 2.535GHz).

After making the model of each path, they are inserted in the schematic on ADS. The simulation of this circuit with connections electromagnetically modeled considers parasitic resistances, capacitances and inductances. New optimizations can be applied to resize components due to correct mismatch and surpass losses.

Due to the re-optimization, some inductors can be increased requiring some changes in layout. When that happens, it is necessary to put the new inductor in the layout, remake some paths and new electromagnetic models. The process of paths modeling and re-optimization is shown in Figure 5.42.

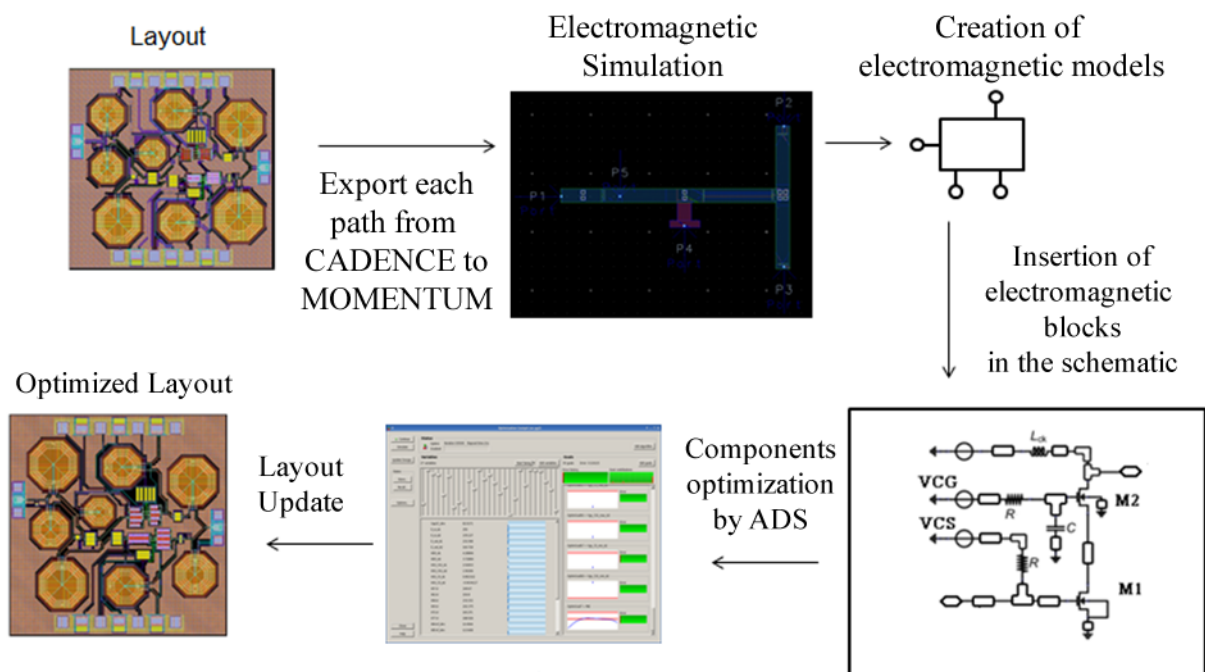


Figure 5.42 – Process of electromagnetic paths modeling and circuit re-optimization

5.4.10.2 Re-optimization Results, Layout Updating and Circuit Description

The re-optimization process applied on the designed DPA caused only a small increase of 3% on layout area (new area 2.99mm^2 , dimensions $1720\mu\text{m}\times 1740\mu\text{m}$) (Figure 5.43) but increased in 6% the PAE performance (absolute value), (26% PAE represents an increase of 30% in relation to 20% PAE) as can be seen in Figure 5.44 [69]. The Figure 5.43 compares new results with the post-layout simulation because it is considered the more precise simulation after the electromagnetic. It can be observed in the gain performance (Figure 5.45) an increase on the small-signal region and a small loss of performance in the high power region. This result shows that the re-optimization not only acted on parasites compensation but it also changed transistors operation point. Nevertheless, the PAE performance considerably increased in level and backoff length.

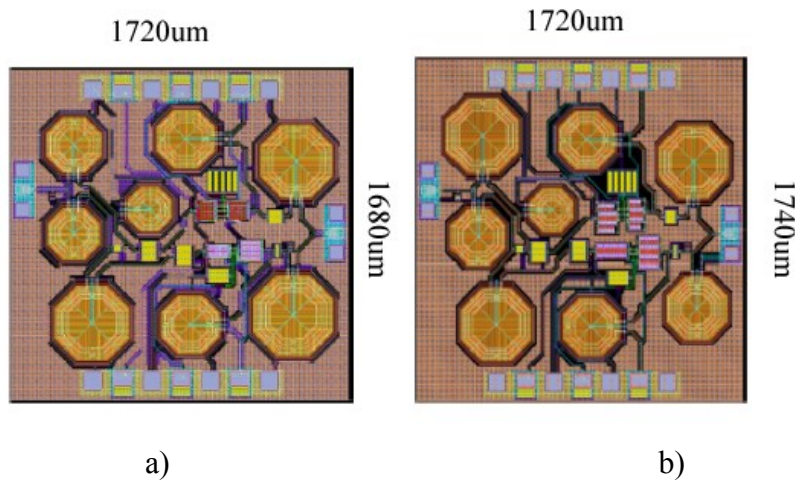


Figure 5.43 – a) Layout before electromagnetic optimization. b) Layout after electromagnetic optimization

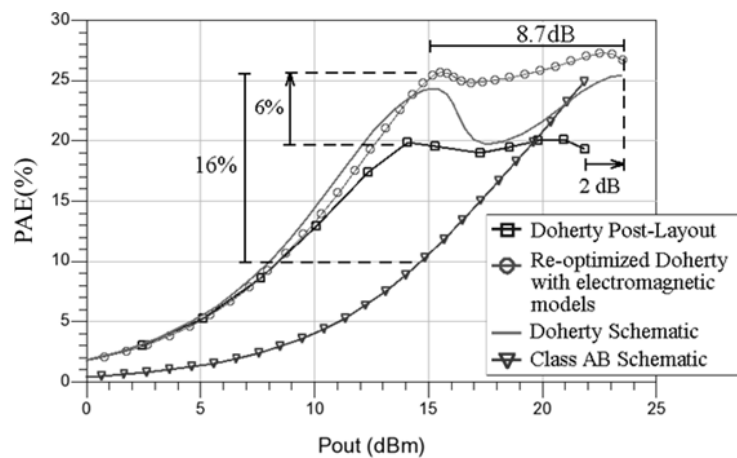


Figure 5.44 – Simulations comparing the PAE between post-layout, schematic and schematic with electromagnetic models from DPA and schematic from a class B PA

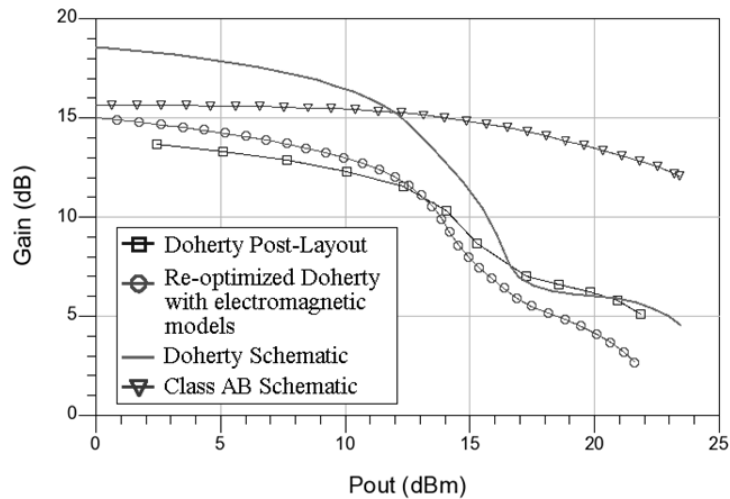


Figure 5.45 - Simulations comparing the gain between post-layout, schematic and schematic with electromagnetic models from DPA and schematic from a class B PA

The re-optimized circuit has the same topology and reference of components of Figure 5.27. Following tables (Table 5.12, Table 5.13, Table 5.14, Table 5.15 e Table 5.16) describe each component.

Table 5.12 – Resistors

Ref. resistor	Individual Value	Dimensions (μm)	
		W	L
R1	1.997 k Ω	5.0	14.12

Table 5.13 – Capacitors

Ref. capacitor	Individual Value	N° of fingers		N° of parallel devices	Total value
		Direction x	Direction y		
C1	4.31 pF	305	150	3	12.93 pF
C2	4.27 pF	454	100	5	21.35 pF
C3	4.14 pF	293	150	2	8.28 pF
C4	1.365 pF	10	148	1	1.365 pF
C5	3.09 pF	33	100	1	3.09 pF
C6	1.78 pF	128	148	1	1.78 pF
C7	4.31 pF	305	150	3	12.93 pF
C8	4.25 pF	452	100	3	12.75 pF
C9	7.61 pF	54	150	2	15.22 pF

Table 5.14 – Inductors

Ref. inductor	Value	N° of turns	Path width (μm)	Diameter (μm)	Length (μm)
L1	4.39 nH	3	11.99	249.954	3117.72
L2	1.57 nH	3	11.99	95.04	1577.64
L3	2.76 nH	3	11.99	165.00	2273.12
L4	4.14 nH	3	11.99	237.59	2994.85
L5	2.55 nH	3	11.99	153.43	2158.2
L6	4.21 nH	3	11.99	240.76	3026.26
L7	2.76 nH	3	11.99	165.00	2273.12
L8	4.38 nH	4	11.99	145.55	3057.37

Table 5.15 – Transistors**

Ref. transistor	Dimensions** (μm)		N° of fingers	N° parallel devices
	W	L		
T1	40.24	0.25	4	22
T2	34.31	0.25	6	29
T3	71.35	0.25	7	27
T4	61.97	0.25	6	22

** The total W total is divided by the number of fingers. For example, W=40 μm and 4 fingers means that each finger has 10 μm length.

Table 5.16 - Polarization

Source	Voltage (V)
VGS_CS_PA1	0,8
VGS_CG_PA1	2,69
VDD_PA1	3,72
VGS_CS_PA2	-0,10
VGS_CG_PA2	2,24
VDD_PA2	4,04

5.4.11 Design Variables Summary

As shown in this chapter, many variables were defined as optimization variable (controlled by optimization methods) and others were manually adjusted due to restrictions on the use of integer variables in a gradient method. Beyond these input variables, performance measures

and voltage limits between transistors pins were also analyzed. The Table 5.17 presents circuit components and their respective number of optimization and manual variables.

Table 5.17 – Number of variables by component type

Type	N° optim. var.	Description	N° manual var.	Description
DC Source	1	Vdc	-	-
RF Source	1	Pin	-	-
MOM Capacitors	1	N° fingers in direction x	1	N° fingers dir. y
Inductors	1	Diameter	1	N° turns
Transistors	2	Width (W), n° parallel devices (M)	1	N° fingers

The Table 5.18 presents the circuit type and its number of optimization and manual variables. Following, Table 5.19 presents a summary of variables and restrictions related to each type of designed circuit.

Table 5.18 – Number of variables by circuit type

Sub-PA			
	N°	N° total var. auto.	N° total var. manual
DC Source	3	3	-
RF Source	1	1	-
MOM Capacitors	3	3	3
Inductors	3	3	3
Transistors	2	4	2
Total	-	14	8
Intermediary DPA			
	N°	N° total var. optim.	N° total var. manual
DC Source	6	6	-
RF Source	1	1	-
MOM Capacitors	13	13	13
Inductors	10	10	10
Transistors	4	8	4
Total	-	38	27
Final DPA			
	N°	N° total var. optim.	N° total var. manual
DC Source	6	6	-
RF Source	1	1	-

MOM Capacitors	9	9	9
Inductors	8	8	8
Transistors	4	8	4
Total	-	32	21

Table 5.19 – Total number of variables in each circuit

Variable Type	Sub-PA	DPA intermediary	Final DPA (reduced networks)
Optimization	14	38	32
Manuals	8	32	21
Performance	3	3	3
Voltage restrictions	15	30	30

5.5 LTE SIGNAL TRANSMISSION

This section presents the distortion information of the designed DPA. Performances after and before the optimization with electromagnetic models were observed and despite of the PAE performance difference, the distortion results were very close due to de similarity of the gain curve of both DPAs.

The AM-AM distortion is mathematically defined as the finite difference of the fundamental component of the output power in relation to the input power. The AM-PM is defined as the finite difference of the phase variation of the fundamental component of the output voltage in relation to the input power. The values of AM-AM and AM-PM distortion are presented in Figure 5.46.

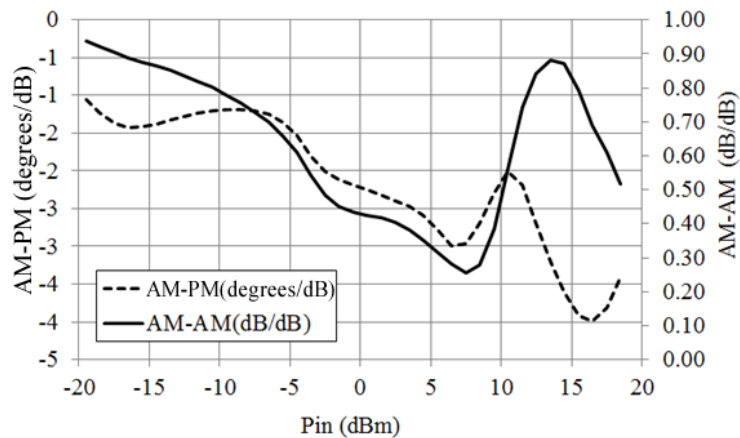


Figure 5.46 – AM-AM and AM-PM distortion curves

The LTE signal simulation was done in ADS using the gain and output signal phase of the DPA, as shown in Figure 5.47. The simplified schematic is presented in Figure 5.48 and the result of the simulation for input power of -10dBm, 0dBm, 10dBm and 19dBm are presented in Figure 5.49. The generation of the LTE signal was done with the component LTE_UL_Src_RF from ADS for uplink simulations with the following parameters:

- Frequency = 2.535 GHz
- Bandwidth = BW 20MHz
- OversamplingOption=Ratio 2
- Resource Block allocation = {0, 100}
- Mapping Type = {1, ... }, where {1} is 16-QAM, for each one of the 10 sub-frames.

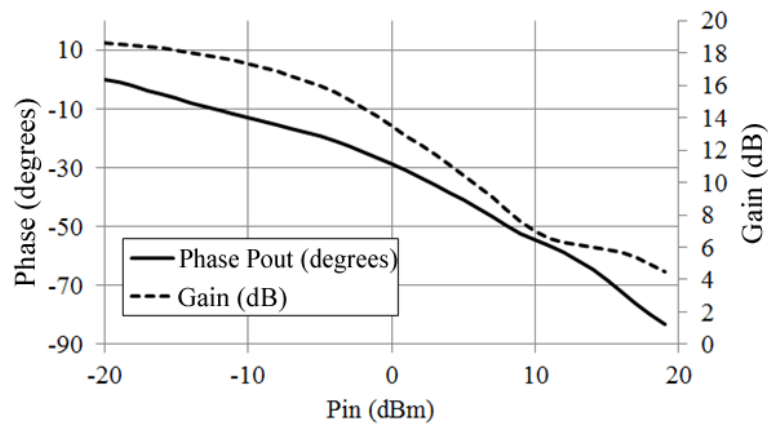


Figure 5.47 – Input data for the LTE signal simulation: gain and output signal phase.

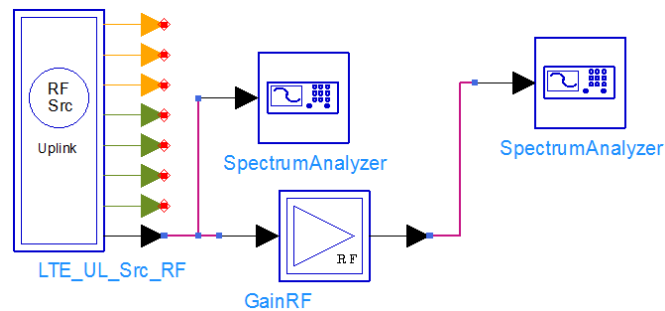


Figure 5.48 – Schematic simulation of the LTE signal in ADS

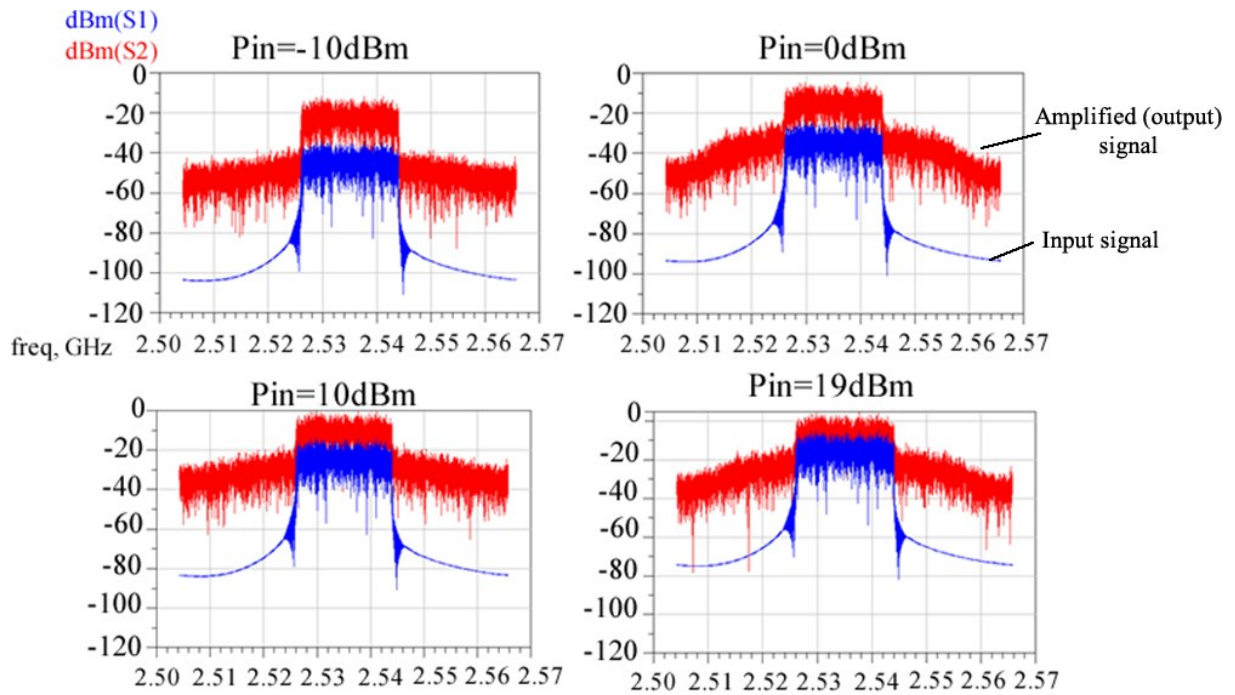


Figure 5.49 – Power spectral density of the input signal (blue) and output signal (red) of the DPA for different input power.

It can be observed in Figure 5.49 that adjacent lobes are not apparent for input power that corresponds to regions that are more linear on the gain curve. Graphs that corresponds to gain compression regions ($P_{in}=0\text{dBm}$ and $P_{in}=19\text{dBm}$) it can be observed the effect of distortion by the apparent adjacent lobes. It is possible to observe on Figure 5.49 the evolution of the gain, being higher on low input power levels and lower when the DPA is already on its compression limit. According to [8] the ACPR on a PA for LTE signals must be less than -30 dB for a linear transmission. It can be observed an ACPR of -25dB for the input power of -10 dBm and an ACPR of -15 dB for the input power of 19dBm, thus, there is a high distortion on the transmitted signal. This result shows that in spite of the favorable PAE performance, the designed DPA needs yet linearization techniques for sending the signal without distortions. The DPA is designed to operate on the high output power region and as the 1dB and the IIP3 compression point are located on the low power region further linearity analysis is not presented.

The distortion on the DPA was already expected due to the strong compression on the high output power region. To make a linear transmission with a non-linear amplifier there are basically three groups techniques to be applied on the PA: feedback linearization [70],

feedforward linearization [65] and signal predistortion [34]. As the signal predistortion technique can be applied on the base band stage or on the RF stage on the low power region there is a negligible impact on the efficiency performance. The predistortion is a well-known technique which has already been applied on DPA as can be seen on [71], [72], [73], [74], [75].

5.6 CONCLUSIONS

This chapter presented a conventional design methodology for integrated PAs and proposed two design methodologies based in optimizations. It was also presented the designed circuits, its component values and layout details. The summary of the number of variables involved on the design demonstrates the exigency level of a DPA design and clarifies the inefficiency of the conventional methodology. It can be seen that the circuit presented a considerable distortion in the LTE amplification due to the non-linearity of the gain, as expected on the moment of the class C PA design. Nevertheless, the DPA presented the desired constant PAE performance that is the fundamental exigency of a DPA.

It can be concluded that PA's design consists on a long and complex task. To implement some topologies, it is imperative for the designer to have appropriate design tools, as for example circuit optimizers. Equations that describe PAs behavior are of great importance for the comprehension of its operation and to guide decisions of the designer. The design of PAs requires specific techniques (as load-pull/source-pull) and many equations in theory are already automatically computed by many types of software that helps the designer (for example, the project of network matching and smith chart computations).

The design and implementation of integrated circuits is a long and expensive process, so, all available tools must be used to foresee with the maximum accuracy the performance that will be measured. The electromagnetic model done by Momentum and HFSS is essential for successfully implement some types of circuits. Optimization techniques, as demonstrated, in some cases are no longer a tool to increase the performance, but, a requisite to reach the functionality.

6 MEASUREMENTS AND RESULTS ANALYSIS

6.1 INTRODUCTION

This chapter starts with the presentation of the fabricated chip, measurements setup and the observed performance. Then, performance analysis and comparisons for schematics, layout and measures are done. Due to the fabrication dates and the stage of the project on the moment, the chip was sent to the Run just after the layout validation, without the re-optimization technique with the electromagnetic modeling.

6.2 THE CHIP AND MEASUREMENTS SETUP

The chip photograph is presented on the Figure 6.1 and measurements setup for the DC polarization and RF signaling is presented on Figure 6.3 and Figure 6.4, respectively.

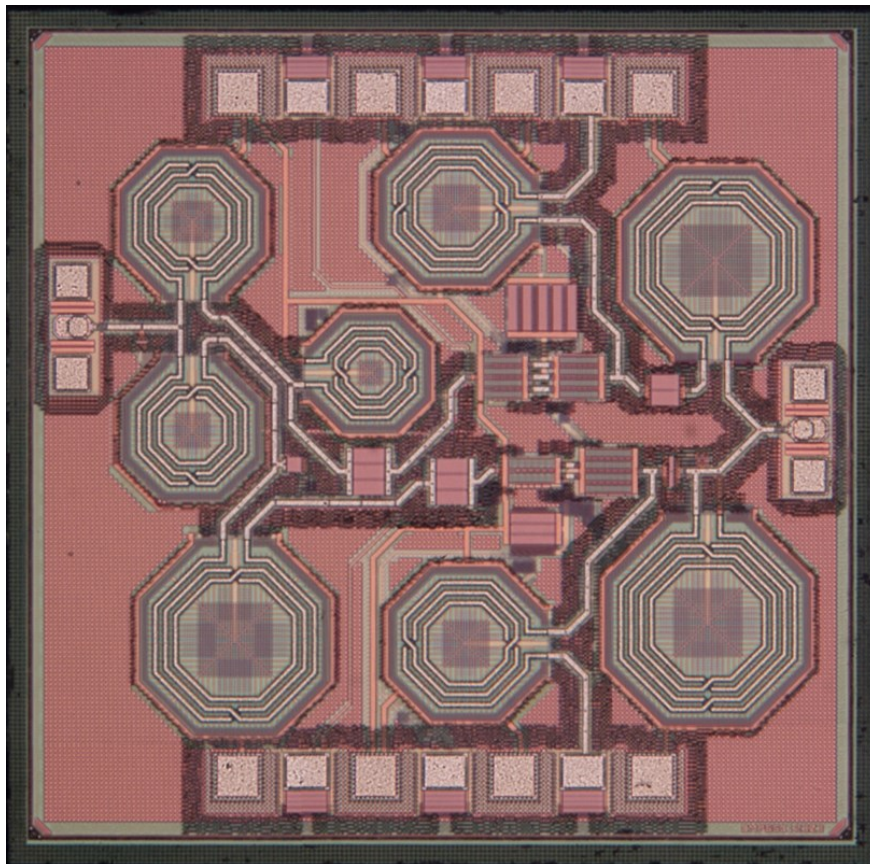


Figure 6.1 – Chip photograph

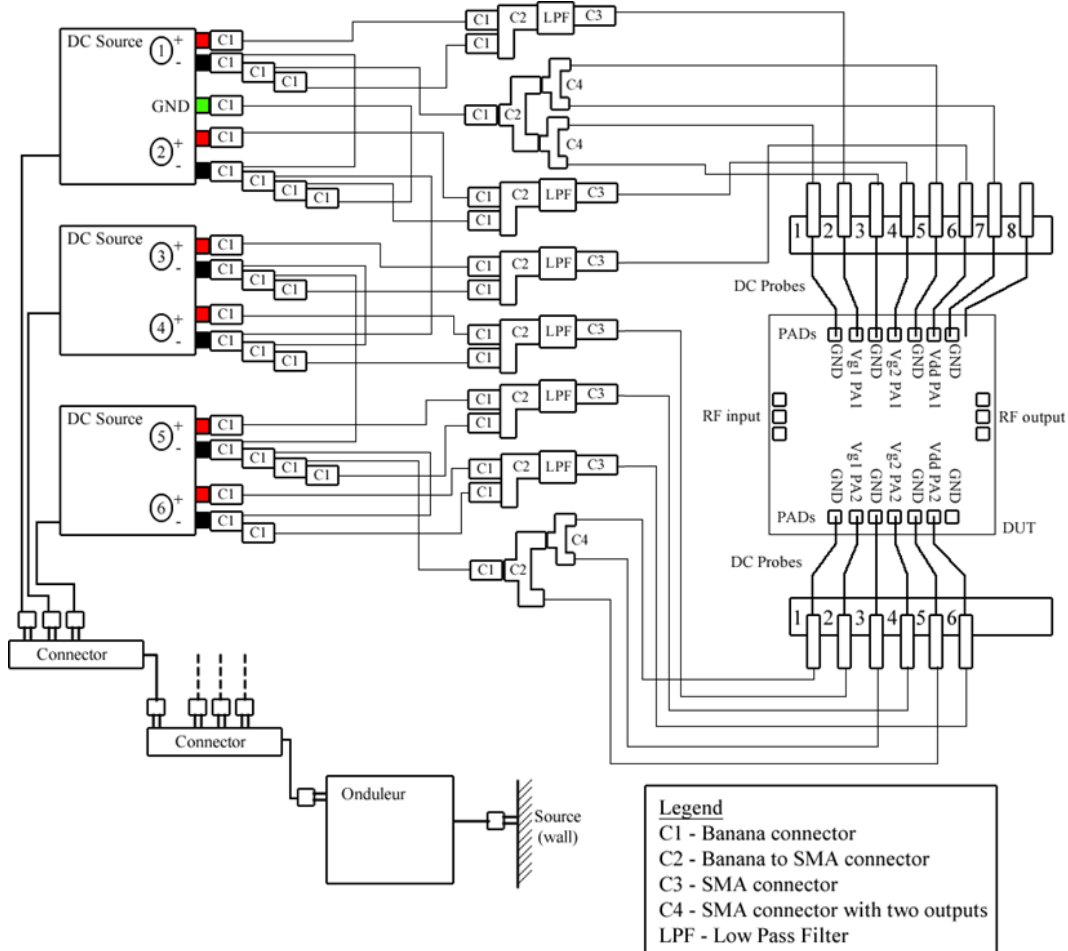


Figure 6.2 – DC polarization setup

The measurements were done with low pass filters (Figure 6.2) connected in each DC polarization to filter improper RF propagation and interference. The Figure 6.3 presents DC polarization sources, microscope and RF pointers.

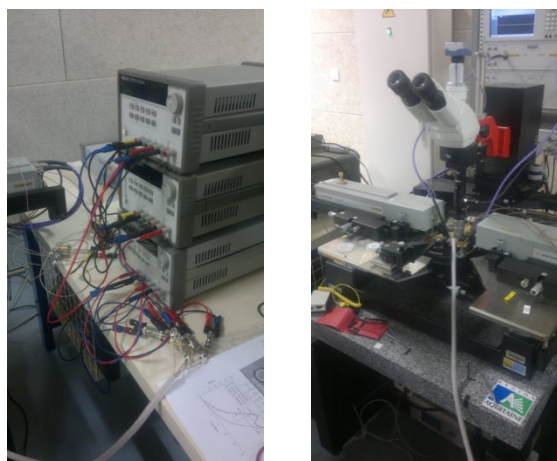


Figure 6.3 – DC sources, cables, connectors (left), microscope and RF pointers (right).

The Figure 6.4 presents the RF setup and Figure 6.5 presents details of devices used on chip polarization. The first component of the RF setup is the RF generator, following, there is a

power amplifier (necessary due to RF generator output power limit), then, the signal reaches the chip with a RF pointer. At the output, there is another RF pointer, an attenuator and a power meter.

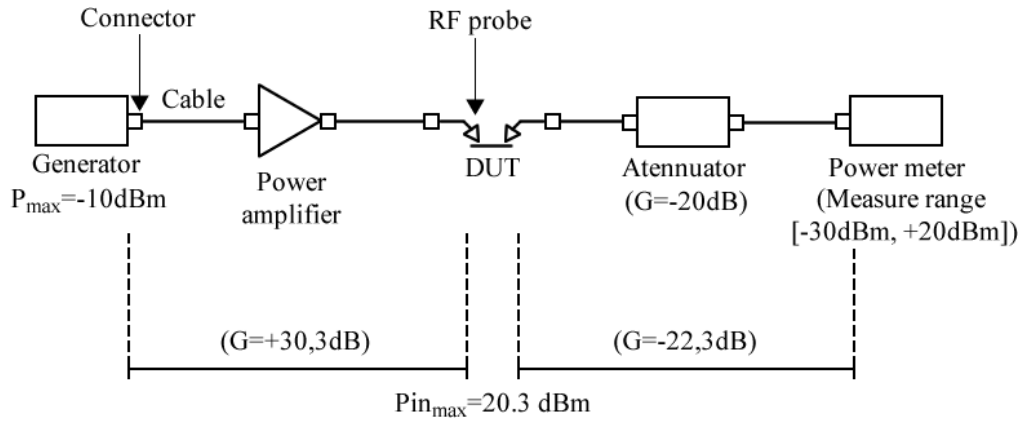


Figure 6.4 – RF setup

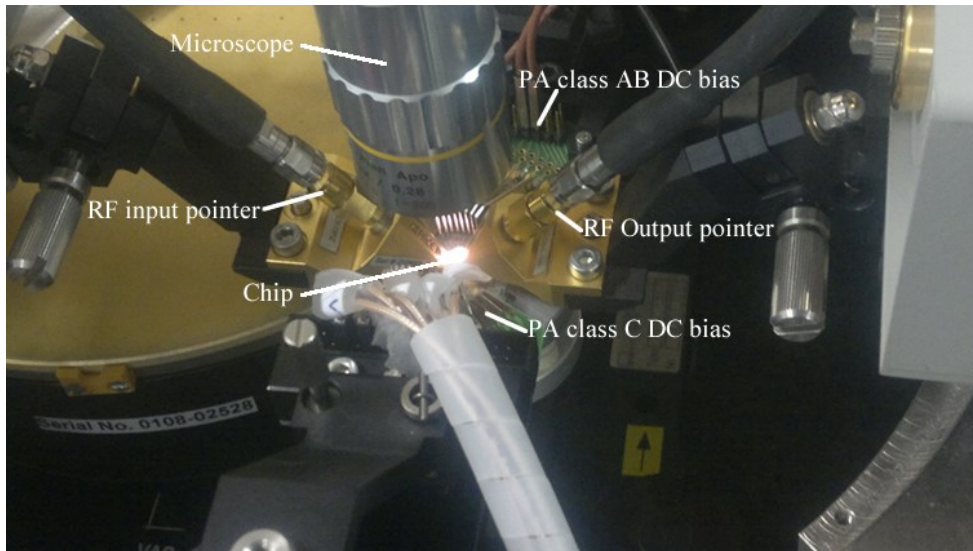


Figure 6.5 – Details of RF and DC polarization setup

Due to the distance between the low pass filters and the chip, long DC polarization cables introduced inductances and resistances that were not considered on simulations. Among these external elements those that caused more impact on the chip performance were the connections on transistor's drains. Inductances and resistances connected on drains of the DPA changes the output matching network producing losses and mismatch. To overcome the mismatch and losses, DC polarization had to be readjusted.

The Table 6.1 presents for each sub-PA the DC drain currents values from simulation and measures when the circuit was biased with the same values from simulation. Table 6.1 shows a good approximation in drain current values from the main PA (class AB), however the

current polarization of the auxiliary PA (class C) was far from the expected value (82 mA) presenting a measured current of 46 mA (43% of difference).

Table 6.1 – Comparing currents from measures and simulations

Polarizations (V)	PA1 – Class AB		Difference	PA2 – Class C		Difference
	Nominal Measure	Simulation		Nominal Measure	Simulation	
Vg_CS	0.8	0.8	0	-0.1	-0.1	0
Vg_CG	2.55	2.55	0	2.36	2.36	0
Vdd	3.21	3.21	0	4.54	4.54	0
IDC(mA) @ maximum output power	80	95	15mA	46	82	36mA

The Table 6.2 presents the optimal polarizations (obtained by adjustments during measurements) and nominal polarizations (values from simulation). DC voltage adjustments were done with the objective to approximate sub-PAs DC drain currents to values from the simulation.

Table 6.2 – Comparing currents and voltages from measures and simulations

Polarizations (V)	PA1 – Class AB		Difference	PA2 – Class C		Difference
	Optimum Measure	Simulation (Nominal)		Optimum Measure	Simulation (Nominal)	
Vg_CS	1	0.8	+0.2	0.2	-0.1	+0.3
Vg_CG	2.8	2.55	+0.25	2.76	2.36	+0.4
VDD	4.22	3.21	+1.01	5	4.54	+0.46
IDC(mA) @ Pout_max*	106	95	11mA	71	82	11mA

* Good approximation.

6.3 MEASUREMENT RESULTS

The Figure 6.6 presents small signal measures with the chip biased with simulation values. It can be observed that the gain is centered near 2.5GHz (design frequency), however its level is of only 6dB, where the expected value was of 15dB, due to the drain current difference presented on the last section.

The Figure 6.7 presents the PAE and the gain performance measured with the chip. It can be observed that the PAE performance has lost the simulated expected shape. It can be seen

some instability on the gains curve on the low power region caused by oscillations in low frequencies that were detected during the measures. The oscillations problem was solved by the filters in each DC polarization and the low level of gain was solved by adjusting the DC current on transistors drains with the same simulated values.

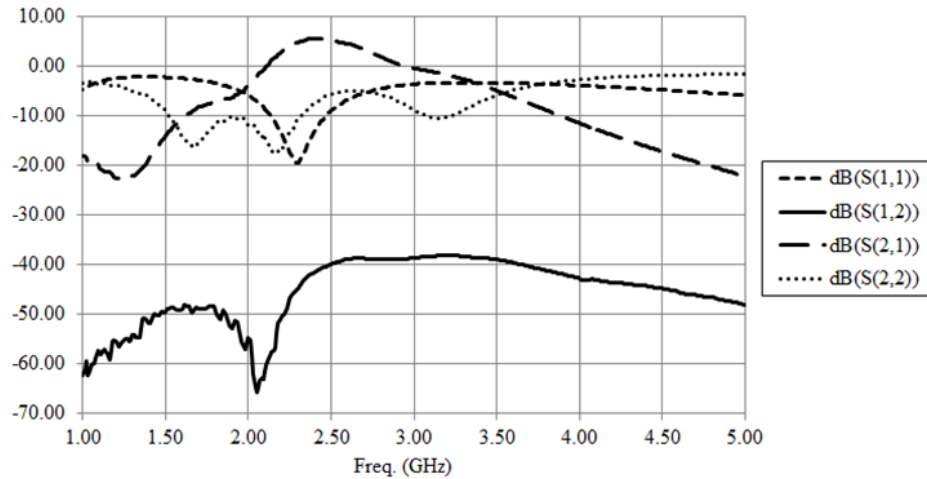


Figure 6.6 – S-parameters measures with the circuit biased with nominal voltages

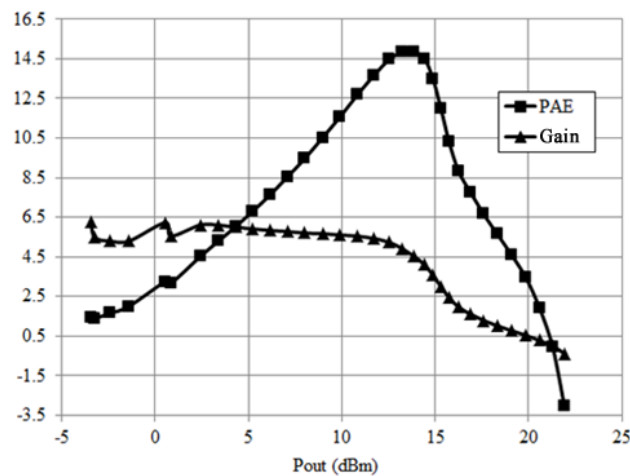


Figure 6.7 – PAE and Gain measures with nominal voltages in 2.5 GHz

The Figure 6.8 presents small signal measures with the chip polarized with optimal voltages and low pass filters in the DC supplies. It can be observed that the expected gain performance was recovered (15 dB) and that it is centered in 2.5 GHz. The Figure 6.9 presents the PAE measures at three different frequencies (2.4 GHz, 2.5 GHz and 2.6 GHz) and the PAE simulated performance of a class B PA schematic. Results show an increase from 8% up to 13% of PAE in the backoff in relation to class B PA. The gain performance presented in Figure 6.10 shows more non-linearity behavior on the DPA in relation to the class B PA due

to the low gain provided by the auxiliary PA (class C), as expected during that stage of the design.

Results show that the objective of producing a constant PAE was reached inside a frequency band of about 200 MHz, which is ten times larger than the largest band demanded by the uplink of the LTE standard (20 MHz). The maximum output power is about 23.5dBm and the PAE constant range is of 7dB, which also satisfies the PAPR of 7.03dB expected by a LTE signal with 16-QAM modulation [9] [7].

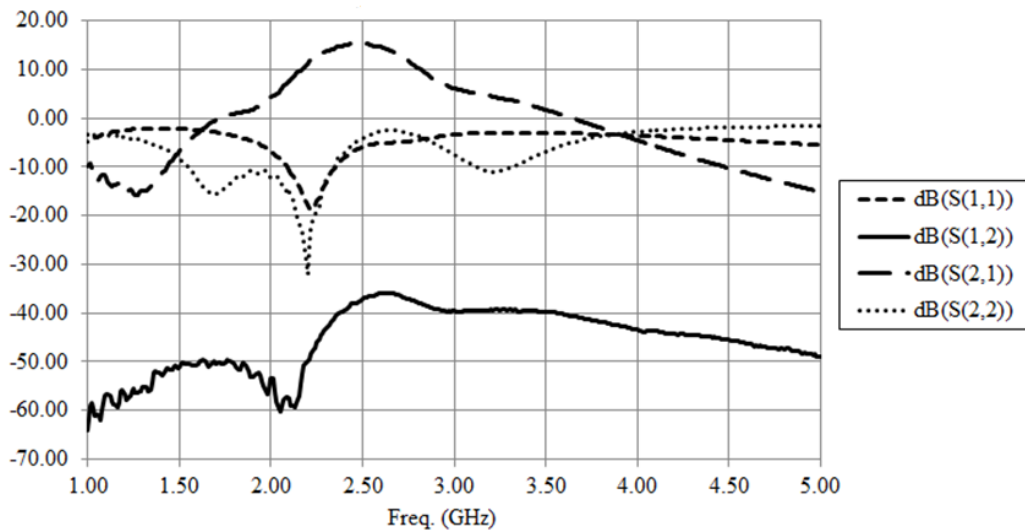


Figure 6.8 – S-parameters measures with the circuit biased with optimal voltages

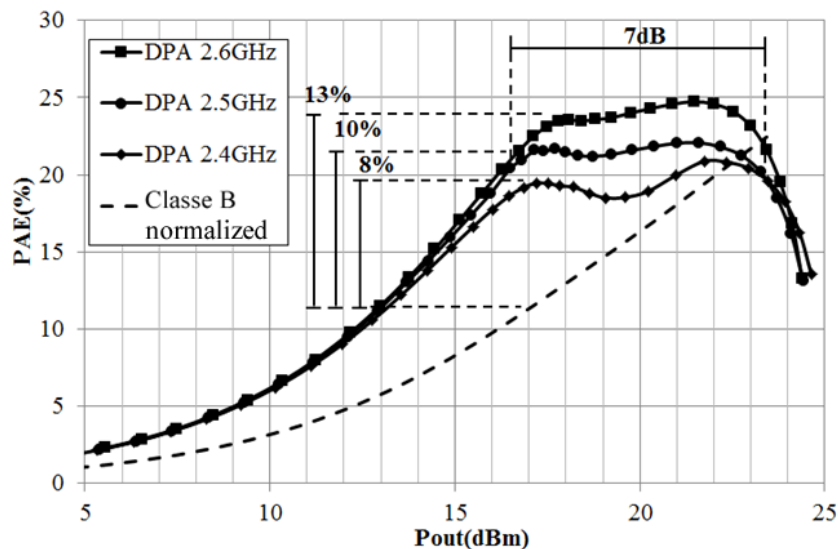


Figure 6.9 – PAE measures with the DPA biased with optimal voltages in 2.4, 2.5 and 2.6GHz and the PAE simulated performance of a class B PA schematic

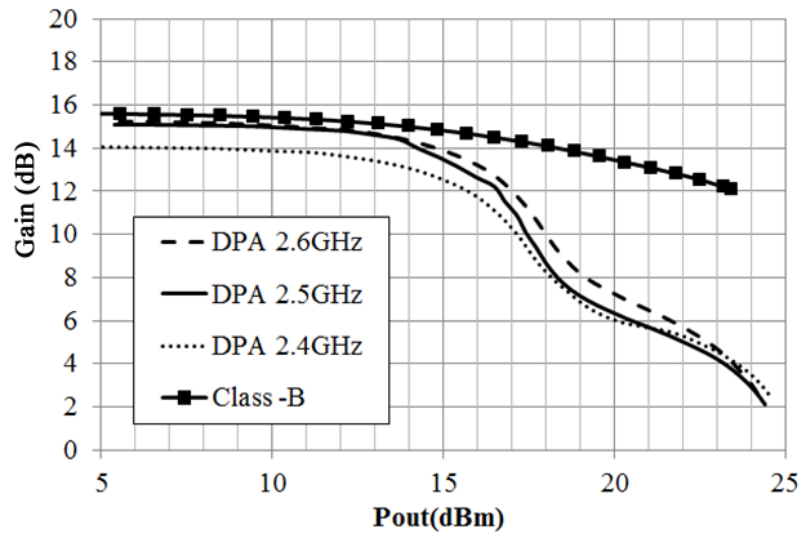


Figure 6.10 – Gain measures for the DPA with optimal voltages in 2.4, 2.5 and 2.6GHz and simulated gain performance of a class B PA schematic

The Figure 6.11 presents measured results in an 8.8dB range of output power (from 14.6dBm to 23.4dBm) in many frequencies, starting from 2.2GHz up to 2.8GHz. It can be observed that the best range of operation is between 2.5GHz and 2.6GHz, which includes the frequency of 2.535GHz of the design.

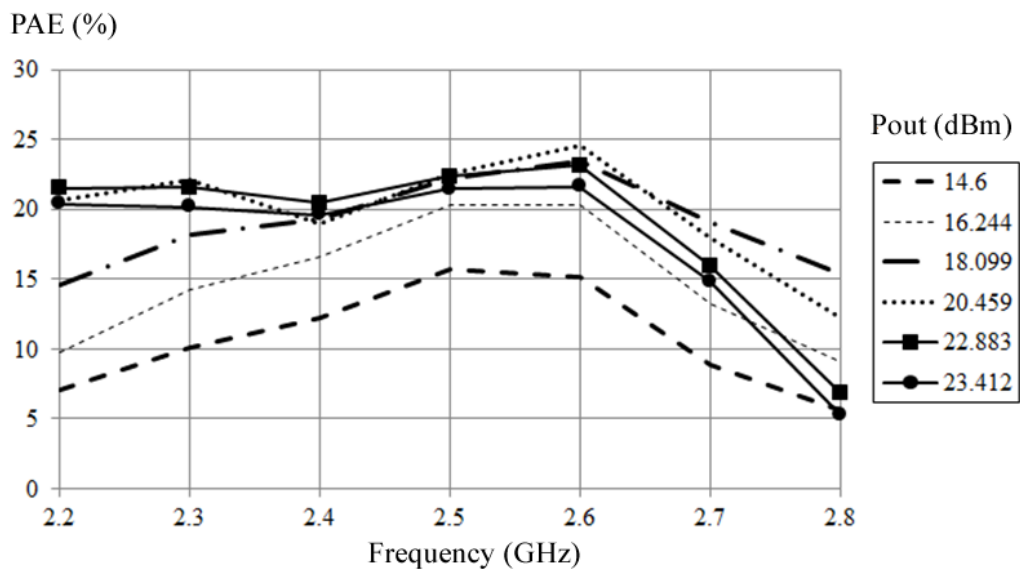


Figure 6.11 – Frequency band measures with DPA biased with optimal voltages

The Figure 6.12 shows that the highest PAE level was measured in the 2.6 GHz frequency and that the PAE performance with the larger backoff and with most constant behavior was in 2.5 GHz. It was observed that with frequency reduction (2.2 GHz curve), the PAE performance of the main PA is decreased, however, the class C PA performance is less affected. Increasing the frequency (2.8 GHz), the class C is more affected than the class AB.

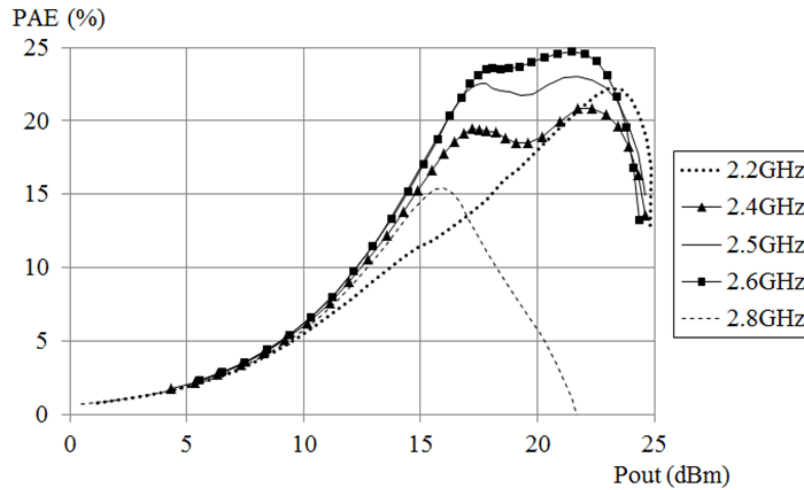


Figure 6.12 – PAE measures with optimal voltages for frequencies between 2.2 GHz and 2.8 GHz.

Measurements with optimal voltages demonstrated that the desired behavior can be produced with the designed circuit even with added inductances and resistances by polarization cables. In an ideal environment, where negligible inductance and resistance are added on drain polarization path, performance variations are expected to be inside Monte Carlo simulation limits, as presented in Figure 5.34.

The designed DPA is a prototype with the objective to be part of a whole integrated RF system. In this case, the environment around the DPA that is composed by DC pads and a guard ring would be replaced by digital circuits for the others RF functional blocks (as mixers, oscillators and others). In this case, the voltage supply connected to the DPA must be properly filtered and stable. As each layout has its own specific issues, the expected variations for the DPA performance can probably change. The best option is to implement a reconfigurable DC supply as can be seen in [32], [76], [77].

6.4 RESULTS ANALYSIS AND COMPARISONS

This section make comparisons between simulated and measured performances for small signal and large signal analysis for the schematic, layout and the chip measured with nominal voltages and optimal voltages.

The Figure 6.13 shows that the small signal gain performance, $S(2,1)$, simulated from the DPA schematic is approximately centered in 2.5 GHz. The curve is not precisely centered in

2.535 GHz, which is not quite important because, as said before, this PA modulates the charge dynamically and the operation region of interest is on the high output power. The S(2,1) presents its better performance in a frequency slightly less than 2.5 GHz differently from the better PAE performance presented in 2.6 GHz in the high power region (Figure 6.12). It can be seen a performance reduction in layout due to unconsidered losses in the schematic, the changes in polarization currents, and it can be also observed that the S(2,1) graph has an offset in direction to a lower frequency. Normally, the frequency reduction on a design is related the increase of capacitances that can be cause by paths and the substrate. However, DPA measurements with nominal voltages present an S(2,1) performance centered on the same frequency of the schematic. It can be noted that approximating the measured drain currents (chip) to the simulated drain currents (schematic) that the measured gain performance also gets near to each other (chip and schematic).

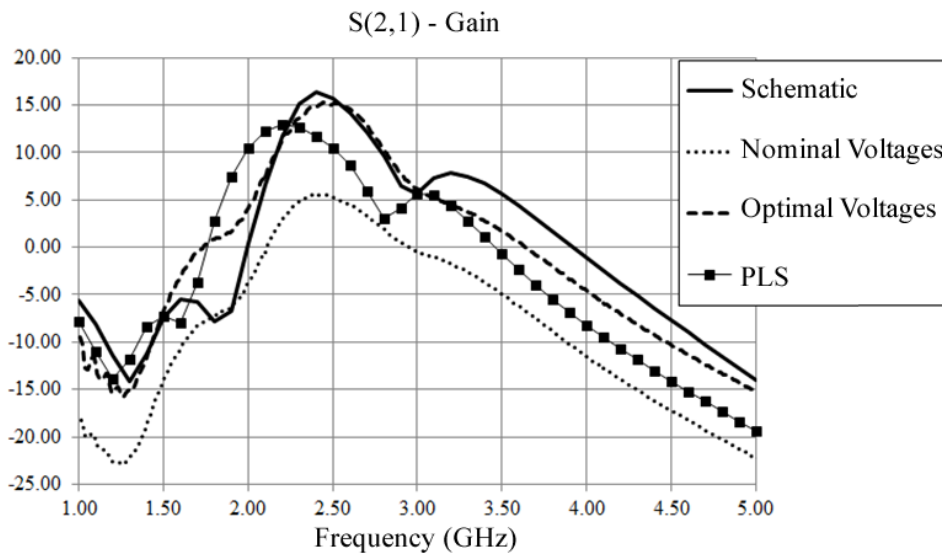


Figure 6.13 – Comparing S(2,1) of schematic simulation, post-layout simulation and measures with nominal and optimal voltages.

Figure 6.14 shows that the S(2,2) performance presents minimal points of the curve of the schematic and measurements (nominal and optimal) centered almost in the same frequency. The Post-Layout Simulation (PLS) performance presents a displacement in relation to other results showing that the parasites extracted from layout changed the impedance matching on the circuit output. Figure 6.14 shows that this displacement was in direction to a lower frequency which indicates that considering parasitic capacitances without considering parasitic inductances a high mismatch can be produced, mainly in a circuit with many long paths and great number of inductors.

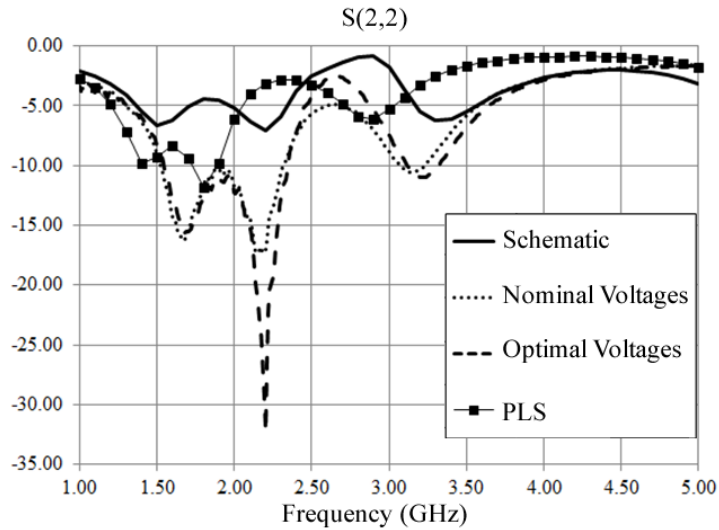


Figure 6.14 – Comparing S(2,2) of schematic simulation, post-layout simulation and measures with nominal and optimal voltages.

The S(1,1) performance in Figure 6.15 shows all curves centered almost in the same frequency, which indicates a good impedance matching at the input comparing simulations and measures. The S(1,2) performance (Figure 6.16) presents a displacement between the PLS and the schematic simulation indicating the presence of parasites in the layout that changed the impedance matching.

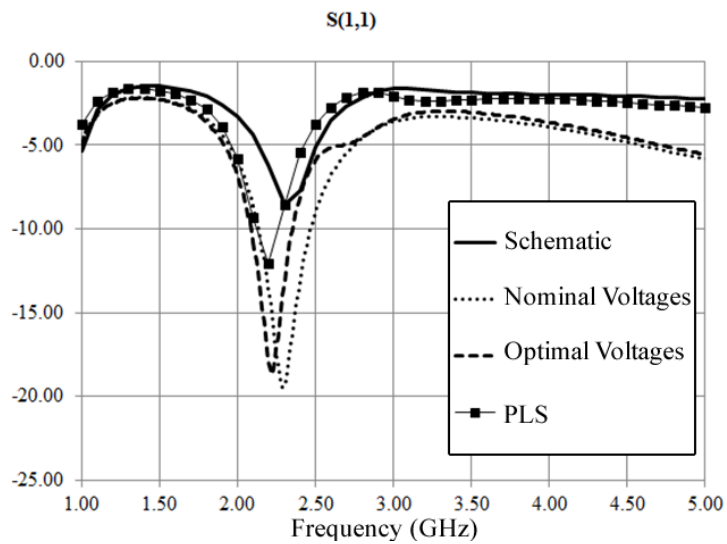


Figure 6.15 - Comparing S(1,1) of schematic simulation, post-layout simulation and measures with nominal and optimal voltages.

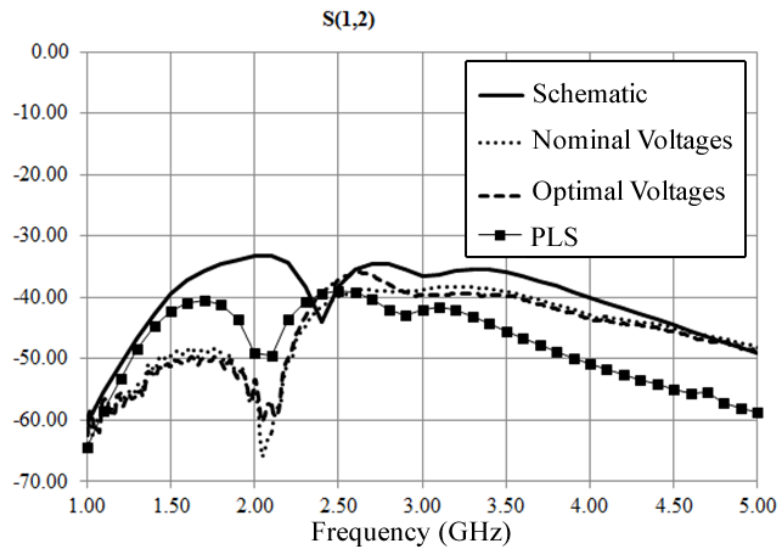


Figure 6.16 - Comparing S(1,2) of schematic simulation, post-layout simulation and measures with nominal and optimal voltages.

The Figure 6.17 presents the PAE performance on schematic and layout simulation and measures with nominal and optimal voltages. Performances from schematic, layout and measures with optimal voltages presented the PAE constant behavior in a large range of output power, in according to Doherty theory. In these curves, it can be observed the two PAE peaks that come from each sub-PA. On the measures with optimal voltages, there was a reduction in the constant PAE region due to the necessity to increase the auxiliary PA gate polarization voltage to correct the DC drain current of the transistor. Due to the compromise between the PAE level and the backoff length (demonstrated on [19] [18]) there was an increase of 2% on the PAE level. The Figure 6.18 shows that in 2.6 GHz there is an increase of 5% on the PAE level, but also a decrease of 2dB in backoff length.

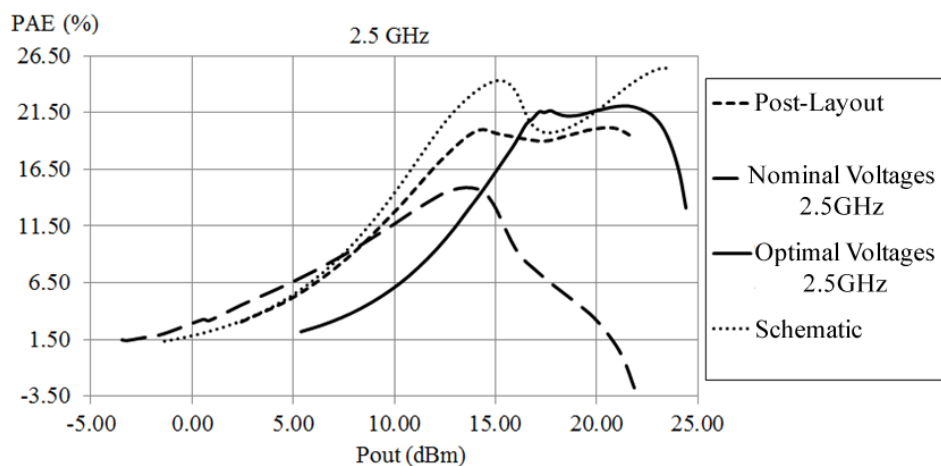


Figure 6.17 – PAE performance of schematic, post-layout and measures in 2.5GHz.

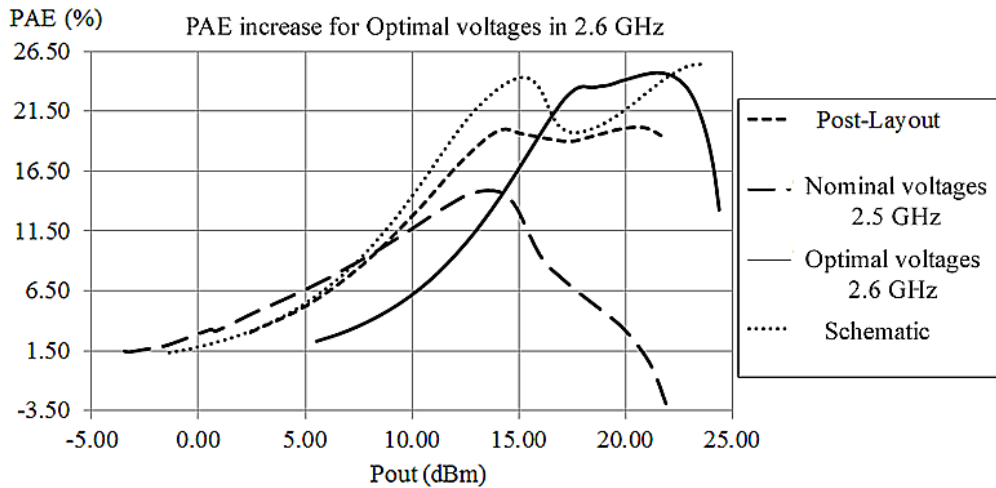


Figure 6.18 – PAE performance of schematic, post-layout and nominal measures in 2.5 GHz and optimal measures in 2.6 GHz.

The post-layout simulation does not consider parasitic inductances, so, it is normal to observe changes between the impedance matching on simulations and on measures. The presented circuit has long paths due to the input and output networks and the size of the inductors. Beyond that, there are eight inductors near to each other, thus, there is the possibility to observe performance changes due to mutual inductive effects between paths and inductors.

Both PLS simulation and schematic with electromagnetic models simulation are important techniques to predict the performance on the measurements, however, both have failures that lead the measured circuit to have a different behavior from simulation. In the case of PLS there is no extraction of parasitic inductances, which leads an imbalance in impedance matching. In the case of electromagnetic simulation, it is not possible to perform the simulation of the ground plane which make impossible to determine with accuracy the resistance and inductance value connected in the source of the transistors. Overcoming these limitations are not easy, on the case of the PLS there are expensive licenses that permits to extract the series parasitic inductances, but not mutual inductances. On the electromagnetic simulation case, we need much higher computational resources. On both cases there is a need for increasing costs and technology.

6.5 SUMMARY OF CHIP PERFORMANCE AND SPECIFICATIONS

To conclude the chip description, Table 6.3 summarizes chip specifications.

Table 6.3 – Project and chip parameters summary

<u>Physic parameters</u>			
Dimensions	1720um x 1680um		
Area	2.9 mm ²		
Package	Without encapsulation. Prototype designed for measurements with probes.		
Metallic environment	Standard chip guard ring		
Magnetic environment	No magnetic protection, no encapsulation		
Power Amplifier Topology	Doherty		
Sub-Amplifiers Topology	Cascode single-ended		
<u>Performance parameters</u>			
Maximum supported input power	19dBm		
Design frequency	2.535GHz		
Band of operation	200MHz (2.4GHz – 2.6GHz)		
Performance (measured)	2.4GHz	2.5GHz	2.6GHz
P _{out,max}	23.5dBm	23.5dBm	23.5dBm
PAE _{max}	20%	22%	25%
Constant PAE backoff	7dB	7dB	7dB
Small signal gain	14dB	15dB	15.5dB
<u>Project parameters</u>			
Technology	CMOS 65nm STMicroelectronics		
Technology options	Standard options 7 metal layers and MOM capacitors		
Integration degree	Fully integrated		

6.6 COMPARISON WITH STATE-OF-ART

Table 6.4 compares the performance of state-of-art of fully integrated DPAs with frequencies near to 2.5GHz designed in 90nm and 65nm CMOS technologies. DPAs in [3] [15] [16] [17] (all for WLAN applications) show a large decrease in performance comparing its PAE value at the maximum output power and at the backoff, and in addition, they do not have resemblance to the constant PAE curve proposed on the theory of Doherty. The DPAs in [3] [15] [17] show only a small increase in the level of PAE compared to class AB/B PAs for a 7 dB backoff. The designed DPA features 10% more PAE than [15] and 5% more than [16], at the same backoff point. Regarding this work, the DPA in [3] and [17] showed almost the same PAE at the backoff, but their efficiency is reduced by 13% and 11%, respectively, compared to its maximum value, approaching a class B PA performance for the same output power.

Published fully integrated DPAs in [3] [16] [17] give a special attention to the linearity of the PA and [15] [3] shows higher gains by using drivers and the differential topology. However, with a Doherty topology, they still present a PAE curve very close of a conventional class B PA, that is, a PAE without the two peaks and the constant range characteristic of a DPA.

Table 6.4 – Comparisons with the state-of-art

Ref.	Freq [GHz]	Gain [dB]	PAE max [%]	PAE @7dB-PBO[%]	Difference PAEmax and PAE@-7dB (backoff)	Psat [dBm]	Tech. [nm]	Topology Details
[15]	3.65	26	35	10	-25	26.5	90	Single ended, cascode, slab inductors
[16]	2.4	17	27	15	-12	20.5	90	Differential, cascode, baluns
[17]	2.4	17	33	22	-11	26.3	90	Differential, cascode, baluns
[3]	2.4	27	34	21	-13	30.5	65	Differential, cascode, baluns, slab inductors
This DPA 2.5GHz	2.5	15.23	22	20	-2	23.26	65	Single ended, cascode, common inductors
This DPA 2.6GHz	2.6	15.23	24.7	22	-2.7	23.42	65	Single ended, cascode, common inductors

The design of a DPA requires two PAs in parallel connected by a large input/output network, therefore, it needs more than twice the area of a conventional PA. The cost of increasing the area must be justified by the PAE increase effect on low/medium power levels, which is the main purpose of a DPA. Furthermore, the use of a class C PA makes the DPA to produce less output power and to have a lower gain. It is more advantageous to use two class AB PAs when designing a PA without efficiency increase in the backoff instead of a class AB and class C. Therefore it is not advantageous to increase chip area, reduce the gain and reduce the maximum output power, without presenting the main feature of a DPA (constant PAE), as shown by the DPAs in [15] [16] [17] [3].

6.7 CONCLUSIONS

This chapter presented the measurement setup and the chip measured performances. Considerable differences were observed between the simulation and the chip biased with nominal voltages due to the insertion of elements not considered in the simulation. The expected performance was recovered by adjusting the bias voltages to provide to transistors the same DC current expected on the simulation.

Next, a comparison was performed with the DPA state-of-art, which demonstrated that the designed chip was able to perform the load modulation proposed by the theory due to the almost constant PAE performance curve with two peaks, unlike last published fully integrated DPAs. The chip presented a constant PAE region suitable for the PAPR of the LTE signal, however, it needs yet linearization techniques to transmit the signal without distortion. This work presents the first fully integrated DPA in 65nm CMOS technology with constant PAE at 2.535GHz focused for signals with high PAPR on mobiles (3G/4G mobile communications).

7 FINAL CONCLUSIONS AND PROPOSALS FOR FUTURE WORKS

The project was focused to the uplink of the last mobile communication standard that is the LTE-Advanced (4G). The motivation was the low efficiency presented by conventional PAs in the low output power region, which reduces mobile battery time when signals with high PAPR are transmitted.

This work started with the DPA bibliographic revision and conventional technique of integration for PAs. Due to problems found on the conventional approach, it was developed a new design methodology based in hybrid and gradient optimizations for designing the sub-PAs of the DPA. Following, sequential optimizations were used to completely integrate the DPA. Beyond allowing the DPA implementation, the proposed methodology makes the PA design more automatic, faster, gives optimized results and more control to PAE performance of the DPA.

Measurements validated the proposed methodology and as result it was designed the first fully integrated DPA in 65nm CMOS technology with constant PAE in a large output power range. The state-of-art revision put into question the feasibility of designing a DPA with almost constant and two peak PAE performance shape, however, this work demonstrated this possibility both in simulations and measurements.

In simulation, it was achieved 25% of PAE with an almost constant level in an 8dB range and an output power of 24dBm. In measurements, it was observed a PAE of 22% in a 7dB range and an output power of 23.5dBm. The chip was designed with only the seven standard metal layers of the technology and MOM capacitors to produce a low cost design.

The DPA implementation in the 65nm CMOS technology permits its integration with other digital circuits, allowing the production of a whole system with the same technology and inside the same chip (SoC). This integration reduces the mobile size due to the reduction of the number of packages. Fewer packages also reduce the losses by eliminating bond wires and package connections with the PCB.

There is yet a need for increasing the gain of the auxiliary PA (class C) for increasing the linearity of the DPA. At the actual state of the chip, it needs linearization techniques to transmit the amplitude modulated signals without distortions.

For future works we propose:

- Increasing the auxiliary PA output power and gain by using the differential topology and a driver between the power splitter and the auxiliary PA.

- Using a PA class E instead of a class C to increase the overall PAE performance and to mitigate the PAE reduction caused by a driver. In 60 GHz applications, inductors can be replaced by transmission lines because of the increased inductive effects on this frequency, which would eliminate the problem of the area increase.

- Designing sub-PAs with the same gain and PAE level due to produce a DPA with both constant gain and PAE at the same range of output power.

- The DPA design for 60 GHz applications would allow integrating the antenna on the chip. In this case, the antenna can be designed with the same output impedance of the transistor, which eliminates the output network matching and reduces PAE and Pout losses.

- Make the DPA input network to match directly to the output impedance of the circuits connected to it. It reduces losses caused by successive adaptations to 50 ohm.

- The 28nm CMOS FD-SOI technology presents an additional layer between the substrate and the transistor, which reduces parasites with the substrate, presents lower leakages, latch-up immunity and allows extra speed for digital circuits in relation to 65nm CMOS bulk technology. This technology also presents less short-channel effects, less threshold voltage variation and back-bias control. The DPA implementation on the 28nm CMOS FD-SOI technology has the potential to increase PAE and output power performance. The 28nm CMOS FD-SOI technology also allows stacking many transistors to increase the supply voltage and output power.

- The GaN technology is also promising for a DPA implementation due to its high PAE performance, high operating voltage and power density, which could reach efficiency values between 50% and 60%. There are also low-cost GaN devices which are grown on sapphire and silicon wafers. GaN's wide bandgap allows for higher breakdown voltages and its thermal conductivity makes it a better substrate than silicon for power amplifier applications.

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ANNEX

ANNEX A – 65NM CMOS STMICROELECTRONICS DESIGN KIT COMPONENTS SETUP FOR THE ADVANCED DESIGN SYSTEM 2009

The 65nm CMOS Design Kit of STMicroelectronics was developed for CADENCE and ADS. In CADENCE, it works perfectly but in ADS some adaptations are needed after the installation for it to work. Today, Agilent provides ADS version 2013, but the DK works only on the version 2009_update1_hotfix20100226 and partially.

On the schematic of simulation the component “*NETLIST INCLUDE*” must be added. In the properties windows of this component (Figure A.7.1) the designer must add references for two files needed to simulate the DK components:

IncludePath=/local_users/ml_cm65n/model_bulk_65nm

IncludeFiles[1]=IMS_65nm_bulk.net

UsePreprocessor=yes

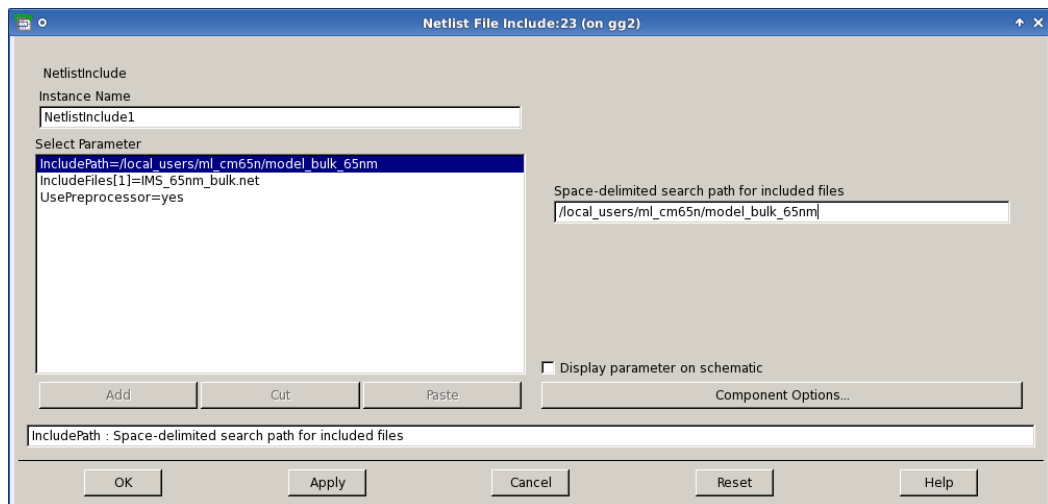


Figure A.7.1 –NETLIST INCLUDE component properties details

The directory referenced by “*IncludePath*” must have the file “*IMS_65nm_bulk.net*” (Figure A.7.3) that is a text file with the following data:

simulator lang=spectre

include “corners.scs”

simulator lang=ads

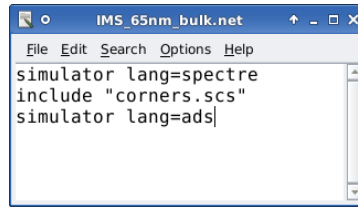


Figure A.7.2– IMS_65nm_bulk.net file

The directory referenced by “*IncludePath*” must have the “*corners.scs*” file (Figure A.7.3) which corresponds to a text file indication simulation parameters and netlist paths of each component used on the circuit. The file used on the project is presented above:

```
//-----
// Process and Mismatch variations selection
// Nov 25 14:22:29 2010
//-----

parameters ext18hv_dev=0
parameters ext18hvADS_dev=0
parameters veriloga_dev=0
parameters mswitch_dev=0
parameters gflag_noisedev_all_cmos065 = 0
parameters gflag_rgateswitch_all_cmos065 = 0

//-----
// Simulation Corners file for simulator spectre scenario default
// ArtistKit 5.6.0.1 (C) STMicroelectronics
// Mar 23 10:46:47 2011
//-----

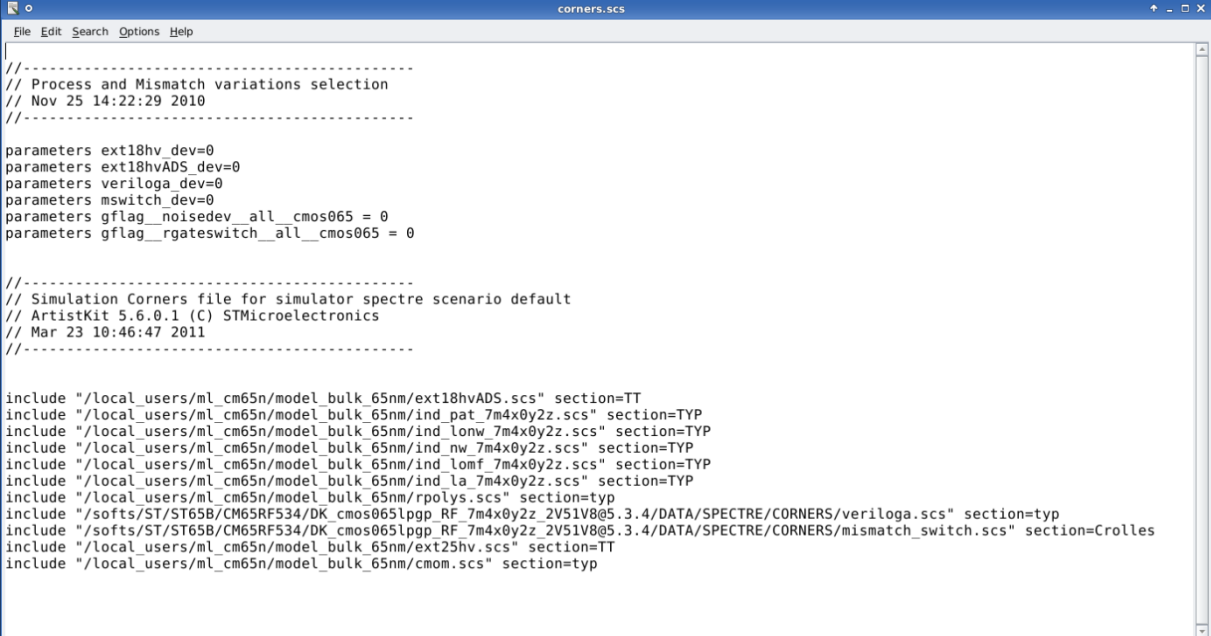
include "/local_users/ml_cm65n/model_bulk_65nm/ext18hvADS.scs" section=TT
include "/local_users/ml_cm65n/model_bulk_65nm/ind_pat_7m4x0y2z.scs" section=TYP
include "/local_users/ml_cm65n/model_bulk_65nm/ind_lonw_7m4x0y2z.scs" section=TYP
include "/local_users/ml_cm65n/model_bulk_65nm/ind_nw_7m4x0y2z.scs" section=TYP
include "/local_users/ml_cm65n/model_bulk_65nm/ind_lomf_7m4x0y2z.scs" section=TYP
include "/local_users/ml_cm65n/model_bulk_65nm/ind_la_7m4x0y2z.scs" section=TYP
include "/local_users/ml_cm65n/model_bulk_65nm/rpolys.scs" section=typ
include
"/softs/ST/ST65B/CM65RF534/DK_cmos065lpgp_RF_7m4x0y2z_2V51V8@5.3.4/DATA/SPECTRE/CORNERS/veriloga.scs"
section=typ
```

include

```
"/softs/ST/ST65B/CM65RF534/DK_cmos065lpgp_RF_7m4x0y2z_2V51V8@5.3.4/DATA/SPECTRE/CORNERS/mismatch_switch.scs" section=Crolles
```

```
include "/local_users/ml_cm65n/model_bulk_65nm/ext25hv.scs" section=TT
```

```
include "/local_users/ml_cm65n/model_bulk_65nm/cmom.scs" section=typ
```



```
File Edit Search Options Help
//-----
// Process and Mismatch variations selection
// Nov 25 14:22:29 2010
//-----

parameters ext18hv dev=0
parameters ext18hvADS_dev=0
parameters veriloga_dev=0
parameters mswitch_dev=0
parameters gflag_noisedev_all_cmos065 = 0
parameters gflag_rgateswitch_all_cmos065 = 0

//-----
// Simulation Corners file for simulator spectre scenario default
// ArtistKit 5.6.0.1 (C) STMicroelectronics
// Mar 23 10:46:47 2011
//-----

include "/local_users/ml_cm65n/model_bulk_65nm/ext18hvADS.scs" section=TT
include "/local_users/ml_cm65n/model_bulk_65nm/ind_pat_7m4x0y2z.scs" section=TYP
include "/local_users/ml_cm65n/model_bulk_65nm/ind_lonw_7m4x0y2z.scs" section=TYP
include "/local_users/ml_cm65n/model_bulk_65nm/ind_nw_7m4x0y2z.scs" section=TYP
include "/local_users/ml_cm65n/model_bulk_65nm/ind_lomf_7m4x0y2z.scs" section=TYP
include "/local_users/ml_cm65n/model_bulk_65nm/ind_la_7m4x0y2z.scs" section=TYP
include "/local_users/ml_cm65n/model_bulk_65nm/rpolys.scs" section=typ
include "/softs/ST/ST65B/CM65RF534/DK_cmos065lpgp_RF_7m4x0y2z_2V51V8@5.3.4/DATA/SPECTRE/CORNERS/veriloga.scs" section=typ
include "/softs/ST/ST65B/CM65RF534/DK_cmos065lpgp_RF_7m4x0y2z_2V51V8@5.3.4/DATA/SPECTRE/CORNERS/mismatch_switch.scs" section=Crolles
include "/local_users/ml_cm65n/model_bulk_65nm/ext25hv.scs" section=TT
include "/local_users/ml_cm65n/model_bulk_65nm/cmom.scs" section=typ
```

Figure A.7.3 – Corners.scs file details

Each component on the design is described by a netlist. The netlist file of the component must be placed on the directory referenced by “*IncludePath*”. To identify which file has the component netlist, the desired component must be added on CADENCE (which doesn’t present DK problems), the proprieties window of the component must be opened and the name on the field “*description*” verified.

The directory referenced by “*IncludePath*” on this project had the following files:

- cmom.scs* – MOM capacitors netlist.
- ext25hv.scs* – Next25 transistors netlist.
- ind_nw_7m4x0y2z.scs* – Inductors netlist.
- rpolys.scs* – Resistors netlist.

These files can be found on the DK directory:

```
...DK_cmos065lpgp_RF_7m4x0y2z_2V51V8@5.3.4/DATA/SPECTRE/CORNERS
```

With these changes the ADS will simulate the circuit with the netlist developed for CADENCE (“*.scs*” extension) instead of the ADS netlists (“*.gem*” extension).

After these changes, each component must be created on ADS. To exemplify this process, the inductor “*indsym_nw*” will be used (all other components follows the same process).

The netlist of the component “*indsym_nw*” is inside the file “*ind_nw_7m4x0y2z.scs*”. Inside the file it can be noted that there are more than one model of inductor:

```
- indsym_nw_7m4x0y2z  
- indsym_nw_7m4x0y2z_acc
```

These models preset different accuracy on the simulation. The chosen model was “*indsym_nw_7m4x0y2z_acc*”. To identify the part of the file “*ind_nw_7m4x0y2z.scs*” that has this model, a search for the text “*subckt indsym_nw_7m4x0y2z_acc*” must be done.

On the line with the text “*subckt indsym_nw_7m4x0y2z_acc*” it is possible to find the pins information:

```
subckt indsym_nw_7m4x0y2z_acc in out sub
```

The pins sequence indicates that they must be referenced as 1 for “*in*”, 2 for “*out*” and 3 for “*sub*”.

Above the line with the model name and pins, there are netlist parameters:

```
subckt indsym_nw_7m4x0y2z_acc in out sub  
parameters  
+ d = xxx  
+ w = xxx  
+ nbturns = xxx  
+ l = xxx  
+ fq = xxx
```

After identifying the exact model name, the sequence of pins and parameters, an ADS schematic must be created and the pins with informations of the netlist must be added, as can be seen in Figure A.7.4.

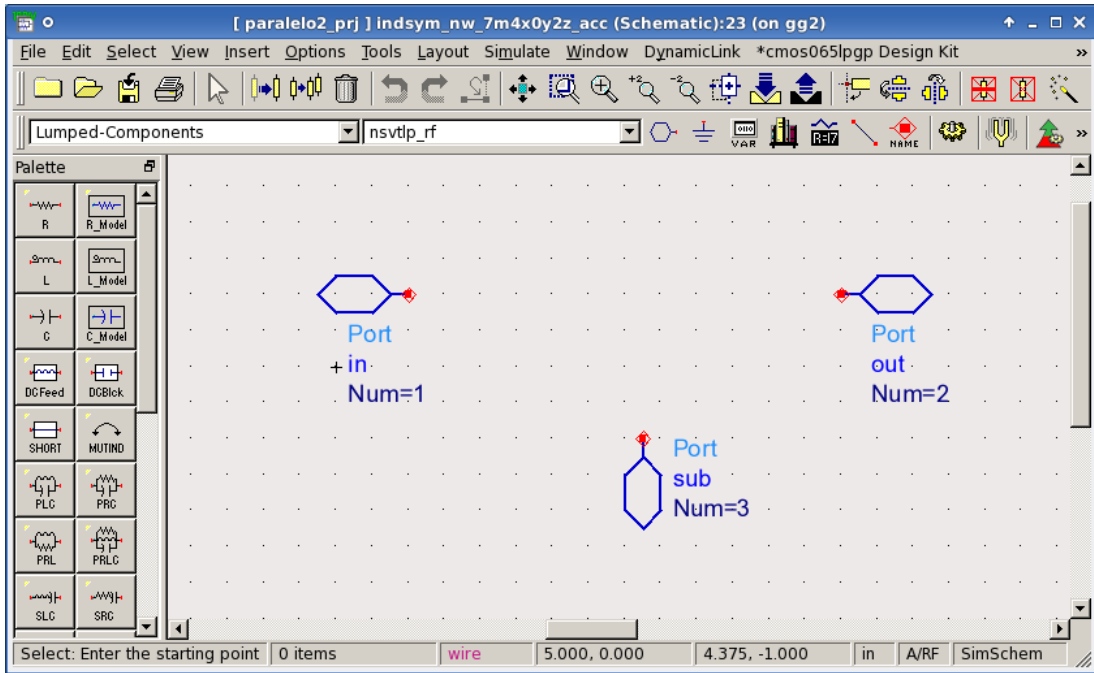


Figure A.7.4 – Component pins details

The schematic that represents the pins of the component must be saved exactly with the same name of the model found on the netlist. For the inductor of the example, the file must be saved with the name “*indsym_nw_7m4x0y2z_acc*”.

Following, the parameters of the component must be added (Files → Design Parameters). On the section “*Parameters*”, the parameters “*d*”, “*w*”, “*nturns*”, “*fq*” must be added (Figure A.7.5).

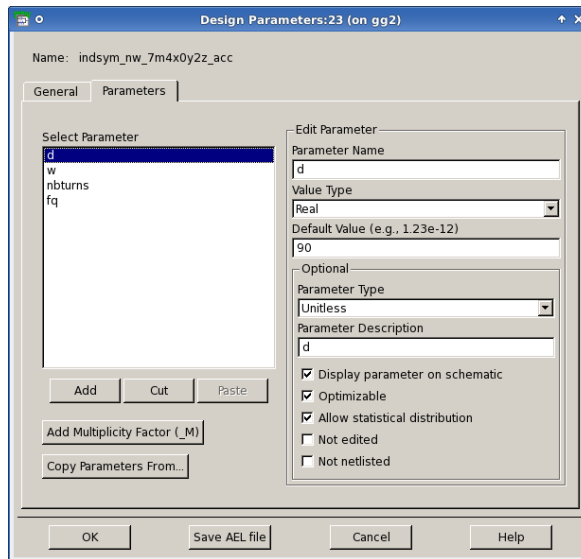


Figure A.7.5 – Detail of the window of component parameters insertion

After creating each pin and defining parameters, a symbol for the component must be created (Figure A.7.6).

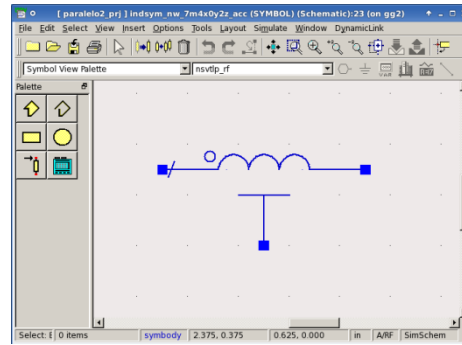


Figure A.7.6 – Component symbol creation

After making all indicated changes, the desired inductor component will be available on the component library.

ANNEX B – CMOS RESTRICTIONS

The evolution of CMOS technology has been very fast since last decade. Its evolution consists on the reduction of the channel length and on the thickness of the insulation on the gate, and as this reduction takes place, design restrictions rise. Main problems related to this type of technology are:

a) Latch-up

The latch-up phenomenon is the creation of a low impedance path resulted from a PNPN parasitic structure that is similar to a thyristor. It can be generated by an accidental creation of this structure among the feeding lines of a circuit with MOSFETs or two transistors positioned very close to each other so that it can shoot the conduction of a current able to make the device to destroy itself.

Although the potential for latch-up is inherent in all CMOS bulk devices (CMOS SOI technology is protected), there are several steps that can be done to reduce the level of latch-up susceptibility in a system as, decoupling the power supply with several 0.01uF to 1uF capacitors on the PCB, using rise time controlled supply, by inserting the supply voltage before signals being able to drive inputs. For layout considerations, a proper ground and power plane should be used in conjunction to decoupling techniques and transient suppression diodes.

b) Quantic confinement and area effect

All nanometric sized materials have a reduced atom chain. In these dimensions there is an offset between absorption and emission of energy that corresponds to the quantic confinement phenomenon. The area effect corresponds to the increase of light emission probability on materials with reduced dimensions, caused by the passage of an electron from excited to non-excited state [25].

c) Short channel effects

When the length of the MOSFET channel have the same magnitude order of the depleting layers of source and drain junctions, the phenomena of short channel appear. In particular, five distinct phenomena can be noticed:

- **Reduction of induced drain barrier or punchthrough:** corresponds to the reduction of the threshold voltage (V_t) when high drain voltages are used.
- **Surface scattering:** corresponds to collisions occurred by accelerated electrons when they move towards the inversion layer. These collisions limit their mobility and it depends on the acceleration caused by the longitudinal electric field that reduces the channel thickness.
- **Speed saturation:** effect that reduces the transconductance when the device is saturated. It also reduces the drain current when its dimensions are reduced without a proportional reduction to its polarization.
- **Impact ionization:** corresponds to the ionization of the silicon atoms inside the channel capable to generate pairs of electrons and holes. This effect reduces the drain current and creates current towards the substrate. This induces the V_t to increase and the G_m transconductance to decrease.
- **Hot electron effect:** highly energized electrons found blocked and eventually accumulate inside the channel. This effect leads to low performance due to the loss of control over the drain current.

Short-channel effects have been mitigated in CMOS devices by the FD-SOI technology, by variations on source and drain structures, as raised source and drain (thin-body MOSFET) which permits more gate control in relation to bulk technologies, by metal source and drain, multiple gate FD-SOI MOSFET.

d) Breakdown voltage

The reduction of the oxide's thickness at the transistor's gate decreases the breakdown voltage [78]. When this voltage is exceeded, a strong current in reverse direction is produced, which can lead to the destruction of the device.

e) Transistor losses and modeling

A significant part of transistor resistive losses are due to connections between its drain, gate and source with circuit paths which are in more superficial metal layers. High currents on parasitic resistances produce large losses, so, they must be considered in the design of a PA.

One of the challenges on PA design is the absence of analytic models adapted to high output power in high frequencies [8]. Normally, transistors models are done in DC or high frequencies only for small signals. Large signal performances are computed by interpolation from DC and small signals. Beyond that, many non-linear effects on CMOS transistors depend from the transistor itself and thermic effects and not to the frequency [8] [79].

f) Metal layers

The technology miniaturization follows the reduction on layers thickness and the reduction of production costs. The 65nm CMOS technology is suitable for digital systems, which have a greater number of transistors than passive components, in opposition to power analogic circuits that need more passive components than transistors and that are more suitable for BiCMOS technologies. The reduced path thickness on 65nm CMOS technology (12.9 μm total thickness for 12 metal layer technology [11]), in relation to other technologies as 250nm, 130nm, reduces the quality factor (Q) of inductors ($3 < Q < 19$) and capacitors and increases the possibility of electromigration. Paths thickness reduction also increases the capacitive coupling between conductive layers and the substrate. Studies [80] demonstrate that the CMOS 65nm substrate presents conductivity capable to realize a considerable impact in the presence of inductors with high currents.

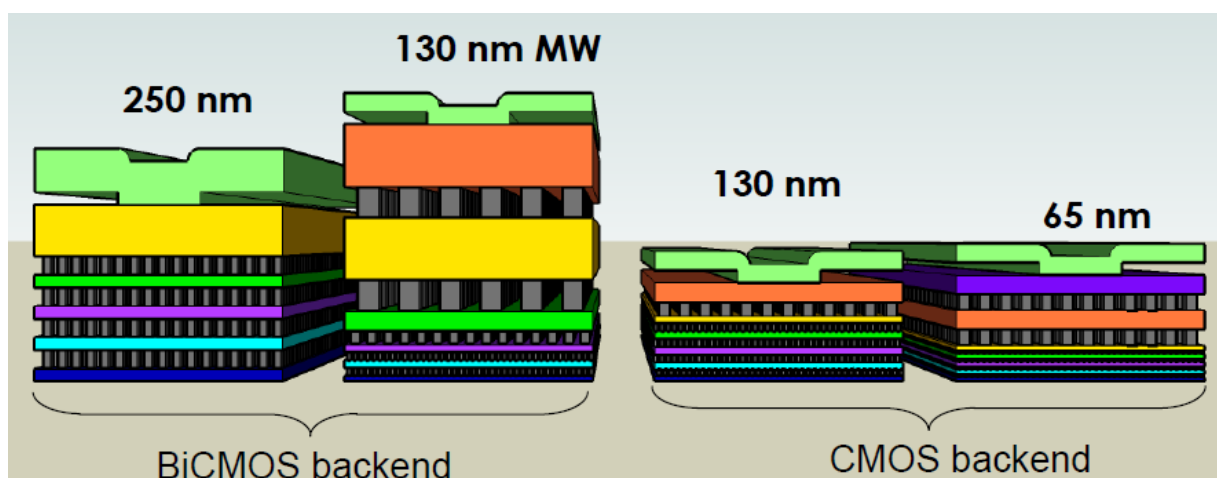


Figure B.1 – Metal layers for different BiCMOS and CMOS technologies [25] [8].